Tektronix, Inc.

Serial ATA International Organization

Version 1.0RC
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Serial ATA Interoperability Program Revision 1.3 Tektronix MOI for PHY, TSG and OOB Tests (Real-Time DSO measurements for Hosts and Devices)

TABLE OF CONTENTS

MODIFICATION RECORD

January 16, 2006 (Version 1.0) INITIAL RELEASE, TO LOGO TF MOI GROUP
Andy Baldman: Initial Template Release

February 2, 2006 (Tektronix Version .9 - beta) INITIAL RELEASE
Kees Propstra, John Calvin, Mike Martin: Phy and TSG MOI Contributions
Eugene Mayevskiy: Tx/Rx Phy MOI Contributions

February 8, 2006 (Tektronix Version .91 - beta)
Kees Propstra, John Calvin, Mike Martin: Phy and TSG MOI Contributions
Eugene Mayevskiy: Tx/Rx Phy MOI Contributions

February 11, 2006 (Tektronix Version .92 RC)
Eugene Mayevskiy: SI01-SI09 Phy MOI Contributions
John Calvin: OOB1-OOB7 MOI Contributions.

February 24 , 2006 (Tektronix Version .93 RC)
Kees Propstra: updated Phy02, TSG01-12
Updated AppendixA
Updated Appendix C: long term freq stability, rise fall and amplitude imbalance, differential skew msmt

March 1 , 2006 (Tektronix Version .94 RC)
Mike Martin: updated OOB test documentation. Minor formatting changes throughout document.

March 31 , 2006 (Tektronix Version .95 RC)
Mike Martin: incorporated reviewer's feedback

April 12 , 2006 (Tektronix Version .96 RC)
Eugene Mayevskiy: incorporated reviewer's feedback (group 2, 4, 6, appendix E)
Kees Propstra: incorporated reviewers' feedback (group 1, 3, 5, appendix A)

May 17, 2006 (Tektronix Version .97 RC)
Eugene Mayevskiy, Mike Martin, Kees Propstra, John Calvin
Incorporated changes to track the IW 1.0 unified test specification as well as reviewers comments.
Added Appendix F for Equivalent Time/ TDNA accuracy parameters
Added Appendix G for Real Time accuracy parameters.

May 25, 2006 (Tektronix Version .98 RC-2)
John Calvin
Incorporated reviewer feedback and broke document into two separate document which separate the RT centric measurements from the ET based ones

May 31, 2006 (Tektronix Version .98 RC-4)
Mike Martin
Incorporated reviewer feedback from SATA Logo conference call review:
PHY-02 : Cleaned up corrupted text – removed bullets 1-4 and associated text.
PHY-04: Corrected test name in discussion section. Corrected deviation formula to show ppm.
All TSG tests: for each test that uses LBP, added directions to inspect waveform for proper disparity.
TSG-02 : removed reference to LFTP. Removed reference to "m" and "x" requirements.
TSG-03 : corrected wording on calculation to include average of the absolute values of the mean for skew1 and skew2. Removed reference to "m" and "x" requirements.
OOB-1: Rewrote test to reflect latest changes in Unified Test Document.
OOB-6: Corrected statement to read "upper limit", rather than "lower limit"
OOB-7: Corrected statement to read "upper limit", rather than "lower limit"
Appendix B : Corrected image corruption and duplicate images.
Appendix C, Section 1: Added wording about using Scope Cursors rather than JIT3 Cursors for making long term frequency stability measurements.
Appendix C, Section 9: Added more detailed information on making differential skew measurement setups.

July 25, 2006 (Tektronix Version .98 RC-5)

Mike Martin
Incorporated reviewer feedback on Phy-02, Phy-03, Phy-04, TSG-01, TSG-02, TSG-03, and OOB-07
Broke up Appendix C, and distributed the text as "Detailed Procedure" in the appropriate test steps to improve readability.
Added legal statement to cover

July 31, 2006 (Tektronix Version .98 RC-6)

Mike Martin
Added Phy-02 content to show higher resolution readings.

August 03, 2006 (Tektronix Version 1.0RC)

Mike Martin
No changes, just 1.0RC version number

September 18, 2006 (Tektronix Version 1.07)

Mike Martin
Replaced DUT with PUT in all instances
Added average measurement technique for PHY-02 and PHY-04
Added HOST changes

September 21, 2006 (Tektronix Version 1.08)

Mike Martin
Rolled to 1.08 as a result of group review
Minor text change to PHY-02 and PHY-04 (removed "mean" on μ line)
Added Gen1 statement to appendix D

September 30, 2006 (Tektronix Version 1.09)

Mike Martin
Rolled to 1.09 as a result of group review
Modified OOB tests to reflect use of AWG7102 generator

January 2. 2007 (Tektronix Revision 1.1, Version 0.91)

Mike Martin
Rolled to new rev/ver numbering scheme
Modified PHY-02 and PHY-04 to use period method
Added Return Loss Verification Procedure

January 16. 2007 (Tektronix Revision 1.1, Version 0.92)

Mike Martin
Modified TSG-06 to show explicit method for measuring mode, and 2nd bit on MFTP.
Modified OOB-01, OOB-06, and OOB-07 to use 2ms record length.
Modified all OOB tests to include Host procedures.
Corrected cable part number 174-4944-00, and added required SW version numbers in appendix A.
Added Scope External Attenuator Setting to Return Loss Verification Procedure

January 23. 2007 (Tektronix Revision 1.1, Version 0.93)

Mike Martin
Modified PHY-01 to use JIT3 for enhanced test efficiency.
Corrected formulas for PHY-02 and PHY-04 to get proper result polarity. Corrected wording on PHY-02 non-SSC to direct use of ref waveform for full resolution.
Modified TSG-02 to use JIT3 for enhanced test efficiency.
Corrected TSG-07 through TSG-10 to reflect UTD changes to test requirements.
Corrected TSG-11 and TSG-12 to incorporate 2nd order PLL.

January 31. 2007 (Tektronix Revision 1.1, Version 0.94)

Mike Martin
Corrected typo in TSG-09, three places where $f_{BAUD}/10$ should have been $f_{BAUD}/500$.

February 1. 2007 (Tektronix Revision 1.1, Version 1.0RC)

Mike Martin
Rolled version for release candidate.

April 11. 2007 (Tektronix Revision 1.1, Version 1.0RC2)

Mike Martin
TSG-02 – Corrected and added detail for 80%/20% setup.
TSG-04 – Added detailed procedure.
TSG-06 – Added "set horizontal pos to 50%" to detailed setup
TSG-07 – Removed reference to Data PLL-TIE2 measurement
TSG-09 – Removed reference to Data PLL-TIE2 measurement
OOB-01 – Replaced screen captures to show only COMRESET/COMINIT. COMWAKE no longer used.
OOB-02 through OOB-05 – corrected to use crst01-3G instead of crst02-3G.
Appendix A – Added reference to new scope models.
Appendix D – Added reference to new scope models.

April 12. 2007 (Tektronix Revision 1.1, Version 1.0)

Mike Martin
Formal release version.
Replaced Logo with trademarked version on cover sheet

October 31. 2007 (Tektronix Revision 1.3, Version .9)

Mike Martin
Modified PHY-02 and PHY-04 to reflect ECN-016.
TSG-07 and TSG-08 – added note that these tests are no longer required per ECN-006
Modified TSG-09 through TSG-12 for ECN-008
Added note in OOB-02 through OOB-05 regarding ECN-17 compliance.
Added Appendix F for AWG7102 calibration of signal amplitude for OOB-01 test
Added Appendix G for ECN-008.

November 9. 2007 (Tektronix Revision 1.3, Version .91)

Mike Martin
Modified PHY-04 to reflect proper limits of +350, -5350 ppm for ECN-016.

January 22. 2008 (Tektronix Revision 1.3, Version .92)

Mike Martin
TSG-05 – corrected final formula to show two result values (per IW scorecard) rather than single value "Max" result
Modified Appendix G to include Gen1 JTF calibration.
Corrected references to SATA 2.6 Spec, and reference tables.
Corrected multiple occurrences of "device" to "PUT"
.

May29. 2008 (Tektronix Revision 1.3, Version 1.0RC)

Mike Martin
Rolled version number to 1.0RC.

ACKNOWLEDGMENTS

The SATA-IO would like to acknowledge the efforts of the following individuals in the development of this test suite.

University of New Hampshire InterOperability Laboratory (UNH-IOL) – Creation of MOI template
Andy Baldman
Dave Woolf

Tektronix, Inc. – Creation of this document
John Calvin
Mike Martin
Kees Propstra
Eugene Mayevskiy

INTRODUCTION

The tests contained in this document are organized in order to simplify the identification of information related to a test, and to facilitate in the actual testing process. Tests are separated into groups, primarily in order to reduce setup time in the lab environment, however the different groups typically also tend to focus on specific aspects of device functionality.

The test definitions themselves are intended to provide a high-level description of the motivation, resources, procedures, and methodologies specific to each test. Formally, each test description contains the following sections:

Purpose

This document outlines precise and specific procedures required to conduct SATA IW UTD ver 1.3 tests. This document covers the following tests which are all Tektronix Real Time DSO based. These tests can be run on either host or drive products.

Test Coverage

PHY GENERAL REQUIREMENTS (PHY 1-4)
PHY TRANSMITTED SIGNAL REQUIREMENTS (TSG 1-12)
PHY OOB REQUIREMENTS (OOB 1-7)

Equipment Preparation

Prior to making any measurements, the following steps must be taken to assure accurate measurements:

1. Allow a minimum of 20 minutes warm-up time for oscilloscope and AWG.

2. Run scope SPC calibration routine. It is necessary to remove all probes from the scope
before running SPC.

3. If using probes, perform the probe calibration defined for the specific probes being used.

4. If using external attenuators to meet the SATA specification for Lab Load on the 50mV range of the scope, follow the procedure outlined in Appendix E.

5. Perform deskew to compensate for skew between measurement channels. Note that it is critical to select “Off” for the “Display Only” control on the Deskew setup window. This will assure that the deskew data is stored with any waveforms that are stored.

PHY GENERAL REQUIREMENTS (PHY 1-4)

Overview:

This group of tests verifies the Phy General Requirements, as defined in Section 2.12 of the SATA Interoperability Unified Test Document, program revision 1.3 (which references the SATA Standard, v2.6).

Test PHY-01 - Unit Interval

Purpose: To verify that the Unit Interval of the PUT's transmitter is within the conformance limit.

References:

[1] SATA Standard, 7.2.1, Table 27 – General Specifications
[2] Ibid, 7.2.2.1.3 – Unit Interval
[3] Ibid, 7.4.11 – SSC Profile
[4] SATA unified test document, 2.10.1

Resource Requirements:

See appendix A

Last Template Modification: April 12, 2006 (Version 1.0)

Discussion:

Reference [1] specifies the general PHY conformance limits for SATA PUTs. This specification includes conformance limits for the mean Unit Interval (UI). Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

In this test, the mean UI value is measured based on the average of at least 100,000 observed UI's, measured at the transmitter output.

Test Setup:

Connect equipment as shown in Appendix B, figure 1 or 2 as appropriate. Note that it is acceptable to use either differential or pseudo-differential (single ended plus math waveform) probes for these measurements.

This test should be done with SSC ON if applicable. If the PUT does not support SSC, a measurement with SSC OFF is acceptable.

Test Procedure:

Using techniques and equipment as described in Appendix A of the SATA Pre-Test MOI, or equivalent, place the PUT in BISTFIS mode transmitting an HFTP pattern. Depending on the capability of the PUT, and the equipment available, it is acceptable to use either BIST-T or BIST-L to produce the needed test pattern.

If the PUT supports disconnects, remove the SATA PRE-TEST system, and connect SATA test fixture. Some PUTs require that the connection not be broken after BIST has been activated. In these situations, it may be necessary to use power splitters to allow simultaneous connection of the PRE-TEST system and the test equipment. Refer to Appendix A of the PRE-TEST MOI for additional details.

Start JIT3 application on Scope. Cancel the Jitter Wizard and within JIT3 recall the setup 'SATA UI rise fall' or 'SATA UI rise fall Ref Wfm'. See the detailed procedure which follows.

This test is performed at both data rates for Gen2 PUTs.

Test pattern(s):	**SATA usage model:**
HFTP	1.5 Gbps and 3Gbps (Gen1i/m and Gen2i/m respectively)

Gen1: 10 us/div, 50 ps/pt (> 100,000 UI)
Gen2: 4 us/div, 25 ps/pt (> 100,000 UI)

Observable Results:

The mean Unit Interval value shall be between 666.4333 ps and 670.2333 ps for 1.5Gbps PUTs, and between 333.2167ps and 335.1167ps for 3.0Gbps PUTs.

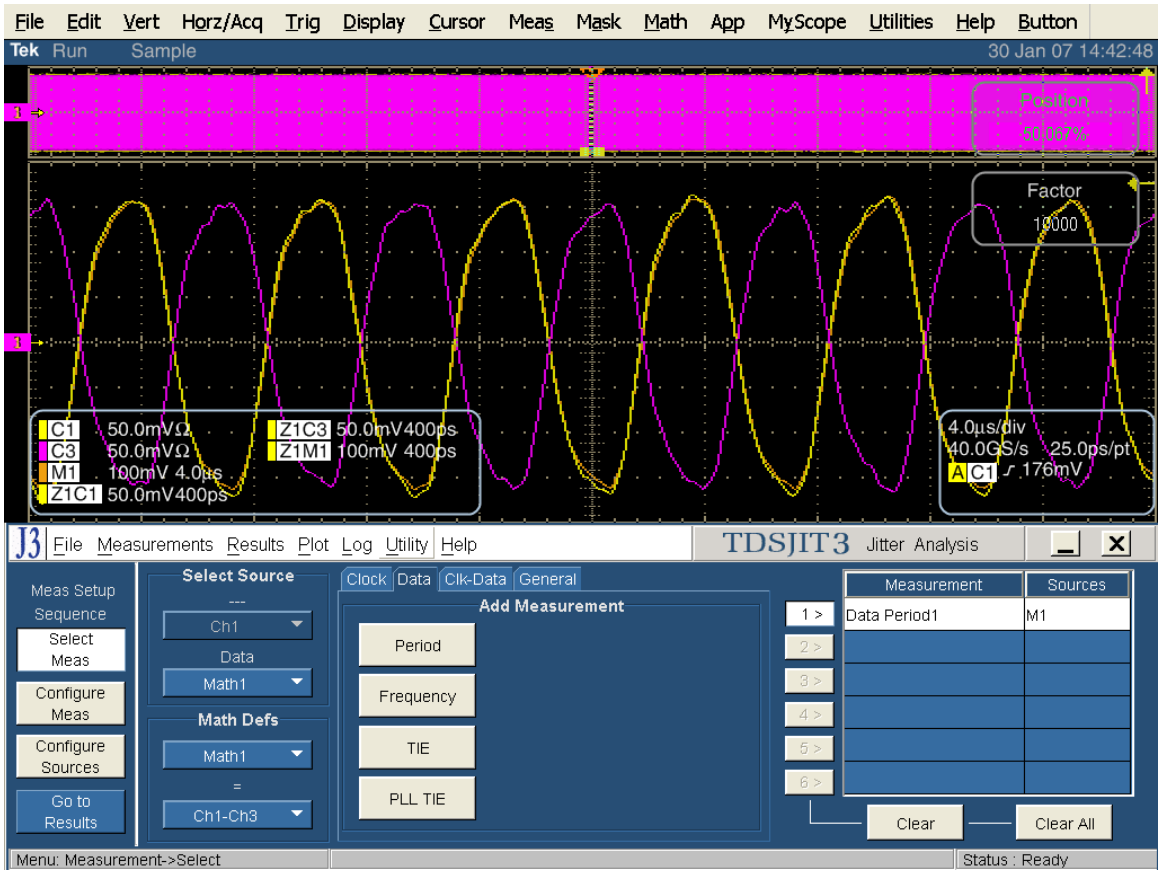
Accuracy: < 3 ps rms

Detailed Procedure:

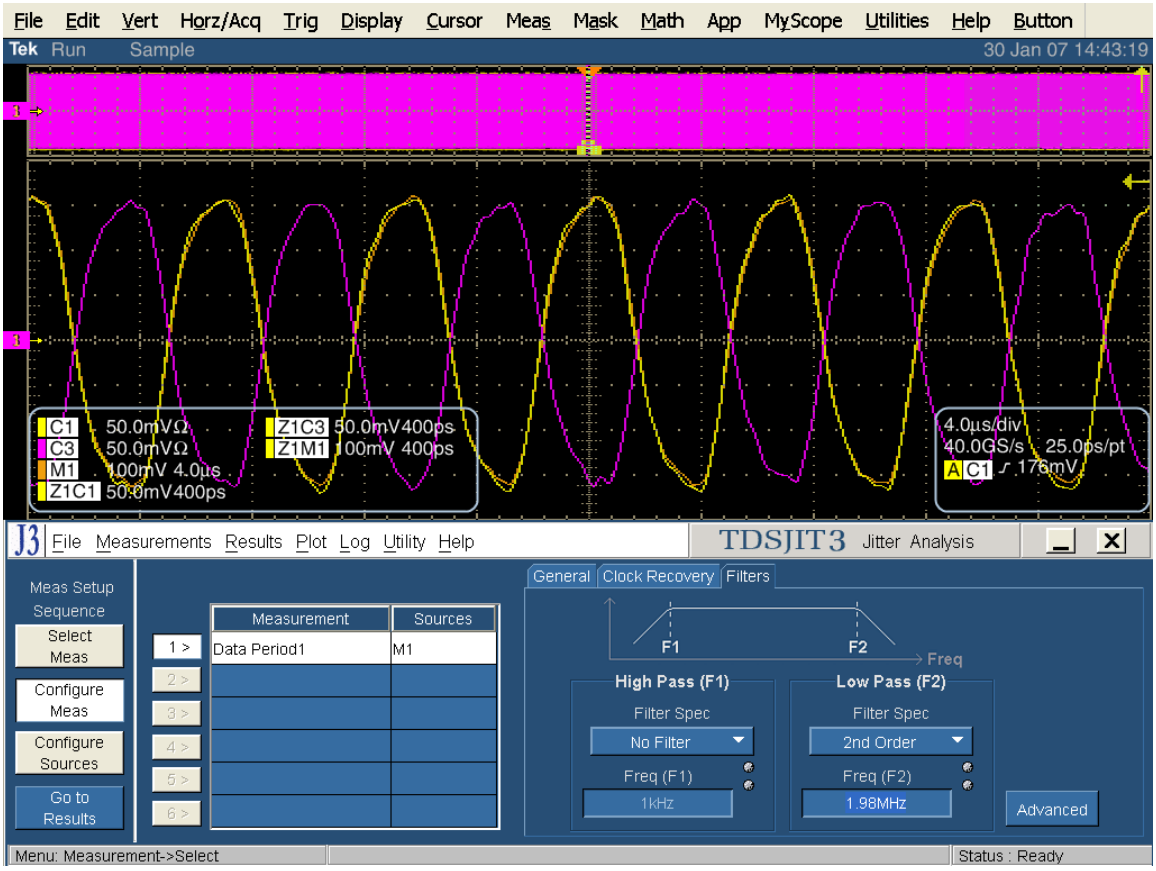
Run JIT3 version 2 by selecting App, Jitter Analysis – Advanced, from the Oscilloscope menu.

Scope setup: 4 us/div, 25 ps/pt

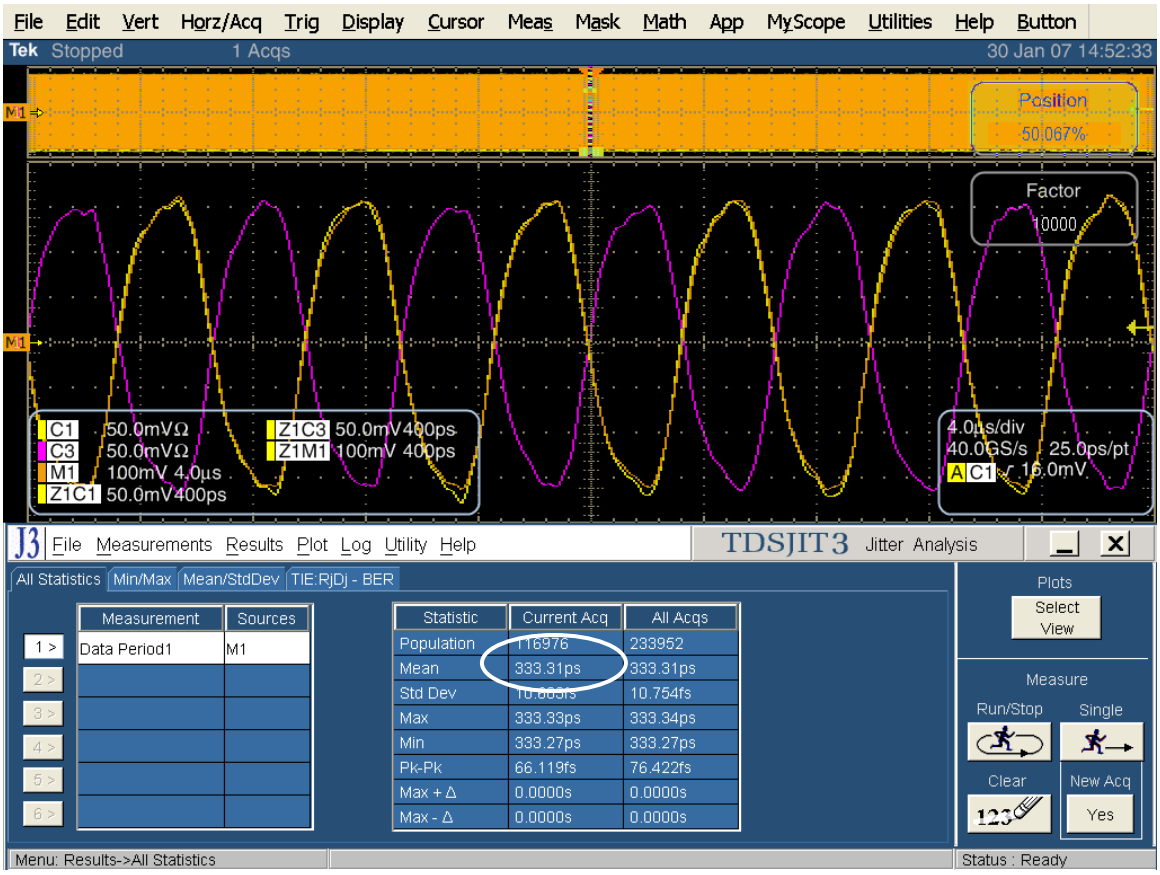
Select Measurement: Data Period on Math1 = Ch1-Ch3.



Configure Measurement: Filters Low Pass second order 1.98 MHz.

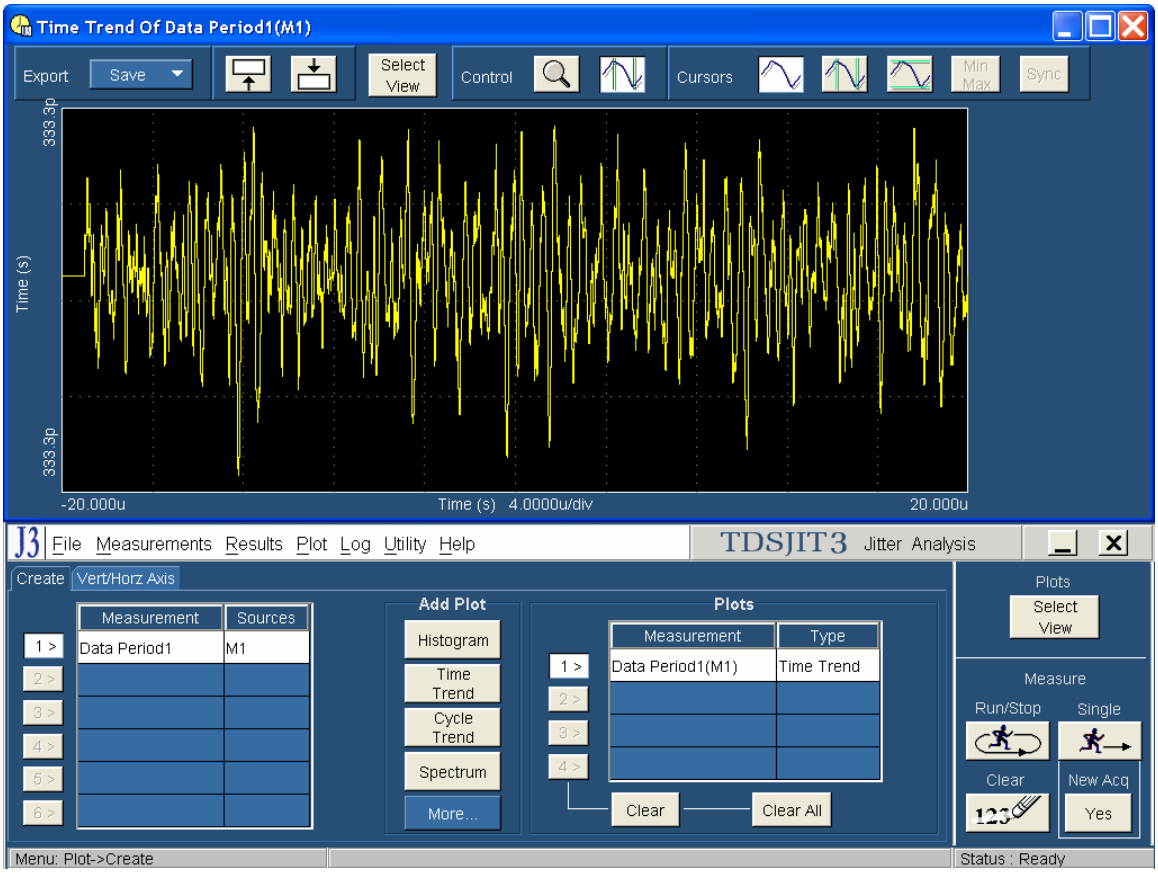


Click on Single to run the application. When complete, the statistics table will contain the results.

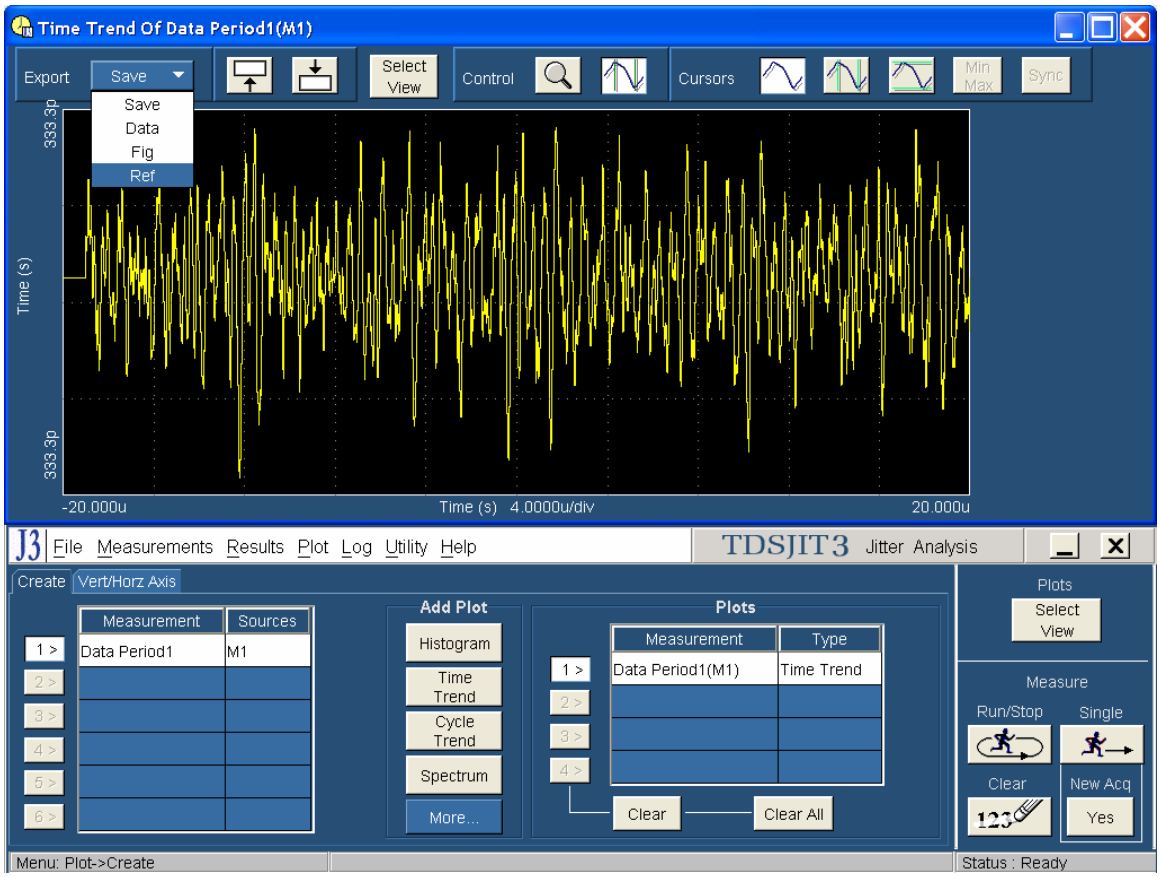


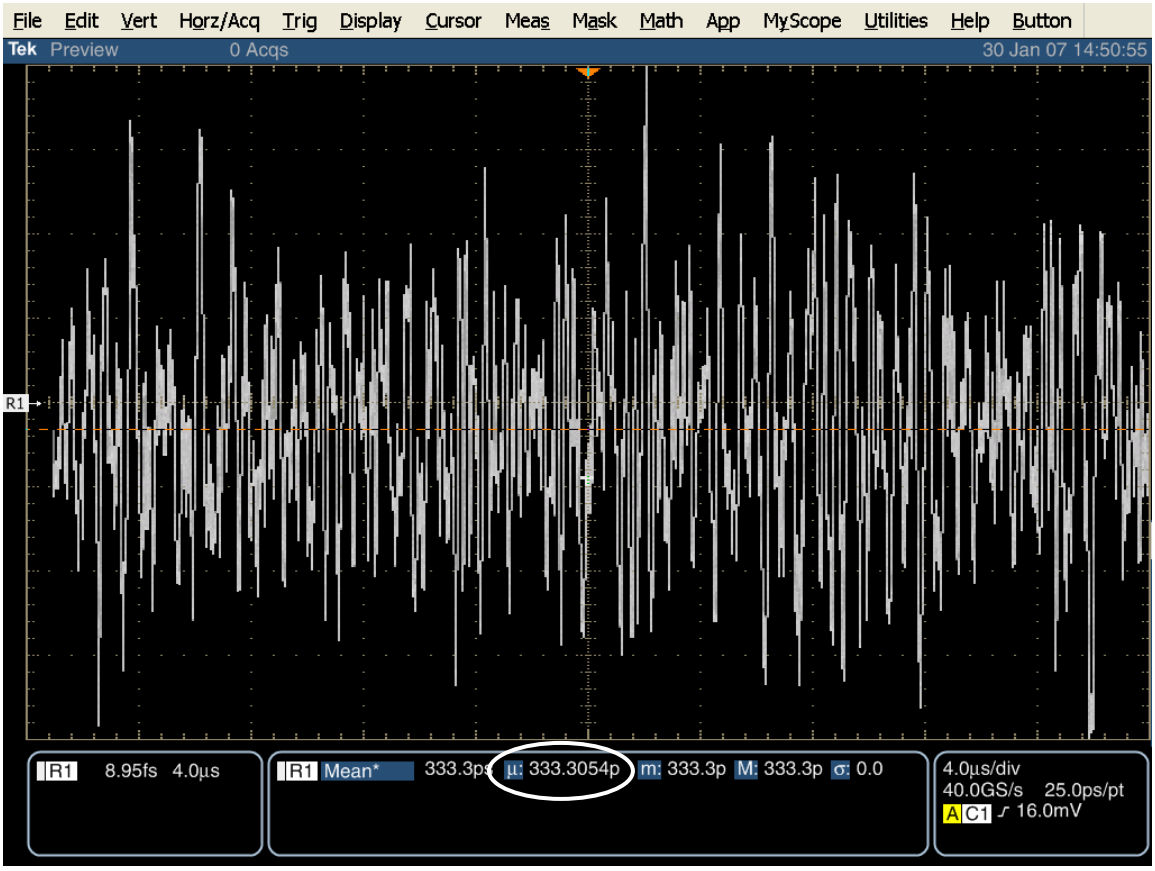
Note that this measurement is rounded up from an internal representation of 9 digits. For measurements that are near the limit, it is possible to use the following procedure to view additional resolution on the measurement.

Select “Plot” from JIT3 main menu bar, and create a time trend plot of the period.



To get more measurement resolution, use the Export: Save function in JIT3's plot screen, and select "Ref" from the pull-down menu. This transfers the Period Profile into the scope's Ref waveform memory.





Once the reference waveform is transferred into the scope's storage, minimize the JIT3 screens, so that only the scope UI is displayed.

Enable Mean amplitude measurement. Despite the fact that these are called amplitude measurements, in this case the measurements will be showing mean period.

Read the value of the current acquisition (ref waveform) following the µ: symbol.

The mean Unit Interval value shall be between 666.4333 ps and 670.2333 ps for 1.5Gbps PUTs, and between 333.2167ps and 335.1167ps for 3.0Gbps PUTs.

Test PHY-02 – Frequency Long Term Stability

Purpose: To verify that the long term frequency stability of the PUT's transmitter is within the conformance limit.

References:

[1] SATA Standard, 7.2.1, Table 27 – General Specifications
[2] Ibid, 7.2.2.1.4 – TX Frequency Long Term Stability
[3] Ibid, 7.4.6 – Long Term Frequency Accuracy
[4] SATA unified test document, 2.10.2

Resource Requirements:

See appendix A.

Last Template Modification: April 12, 2006 (Version 1.0)

Discussion:

Reference [1] specifies the general PHY conformance limits for SATA PUTs. This specification includes conformance limits for the TX Frequency Long Term Stability. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

Note: Per ECN-016, this test is now only performed on PUTs that DO NOT have SSC enabled.

Test Setup:

Connect equipment as shown in Appendix B, figure 1 or 2 as appropriate. Note that it is acceptable to use either differential or pseudo-differential (single ended plus math waveform) probes for these measurements.

Test Procedure:

Using techniques and equipment as described in Appendix A of the PRE-TEST MOI, or equivalent, place the PUT in BISTFIS mode transmitting an HFTP pattern. Depending on the capability of the PUT, and the equipment available, it is acceptable to use either BIST-T or BIST-L to produce the needed test pattern.

If the PUT supports disconnects, remove the SATA PRE-TEST system, and connect SATA test fixture. Some PUTs require that the connection not be broken after BIST has been activated. In these situations, it may be necessary to use power splitters to allow simultaneous connection of the PRE-TEST system and the test equipment. Refer to Appendix A of the PRE-TEST MOI for additional details.

Start JIT3 application on Scope. Cancel the Jitter Wizard and within JIT3 recall the setup 'SATA SSC and LTF' or 'SATA SSC and LTF Ref Wfm'. See the detailed procedure which follows.

This test is performed once at fastest data rate for the PUT.

Test pattern(s):	**SATA usage model:**
HFTP	1.5 Gbps and 3Gbps (Gen1i/m and Gen2i/m respectively)

40 us/div (> 10 SSC periods), 25 ps/pt

Plot period v.s. time.
Record the maximum frequencies in the profile, using cursors.

Observable Results

The Frequency Long Term Stability value shall be between +/- 350ppm for both 1.5Gbps and 3.0Gbps PUTs.

NON-SSC:
Record the average ppm value.

Accuracy: +/- 2 ppm

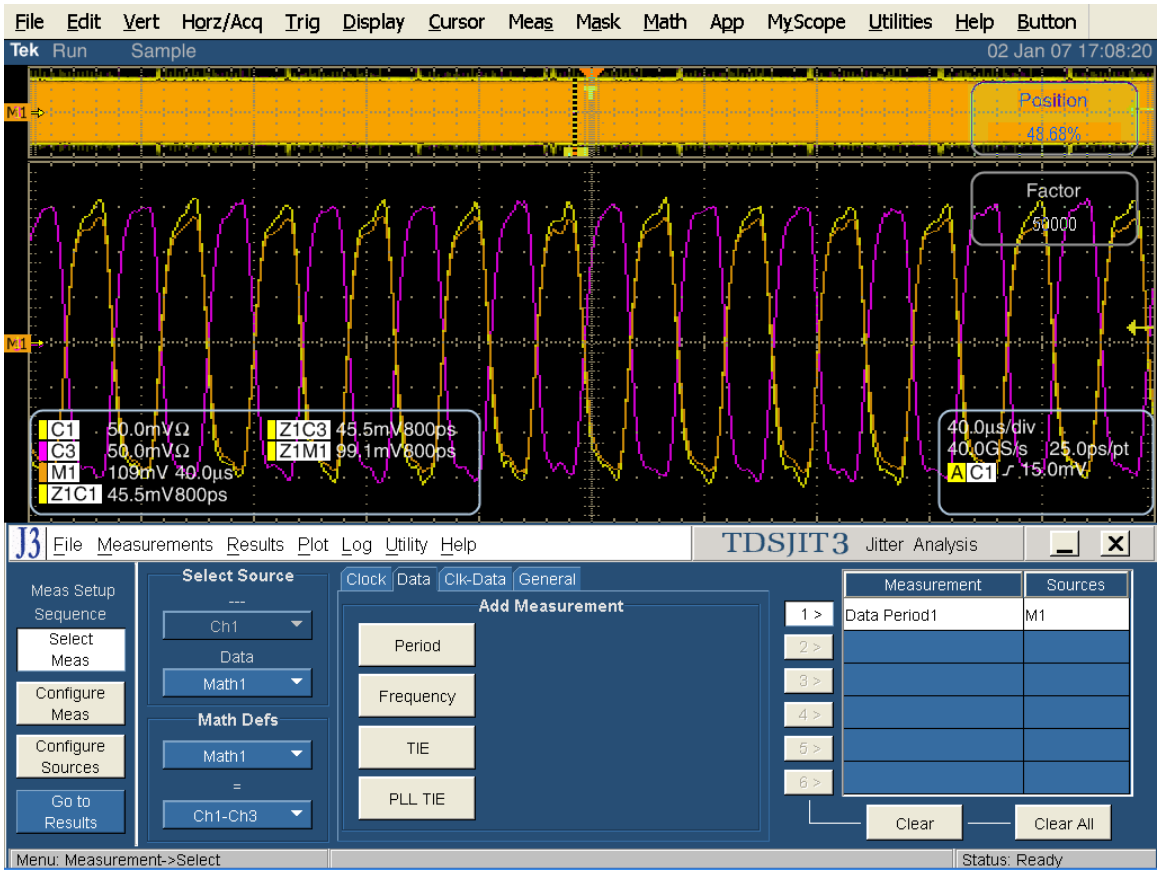
Possible Problems:
Section 7.4.11 of the SATA specification (version 2.5) requires the use of a low pass filter that is 60 times greater than the modulation frequency of the SSC. This equates to a 1.98MHz low pass filter for a 33kHz SSC. On some systems, the SSC profile may present a lot of noise as the cycle reaches its maximum frequency. For diagnostic purposes, it may be useful to reduce the filter from 1.98MHz to 1MHz (or even down to 300kHz in extreme cases). The new value should be selected to get a cleaner period time trend without changing the SSC modulation depth and frequency. Note that the altered setting is not valid for compliance tests.

Detailed Procedure:

Run JIT3 version 2 by selecting App, Jitter Analysis – Advanced, from the Oscilloscope menu.

Scope setup: 40 us/div (>10 SSC periods), 25 ps/pt

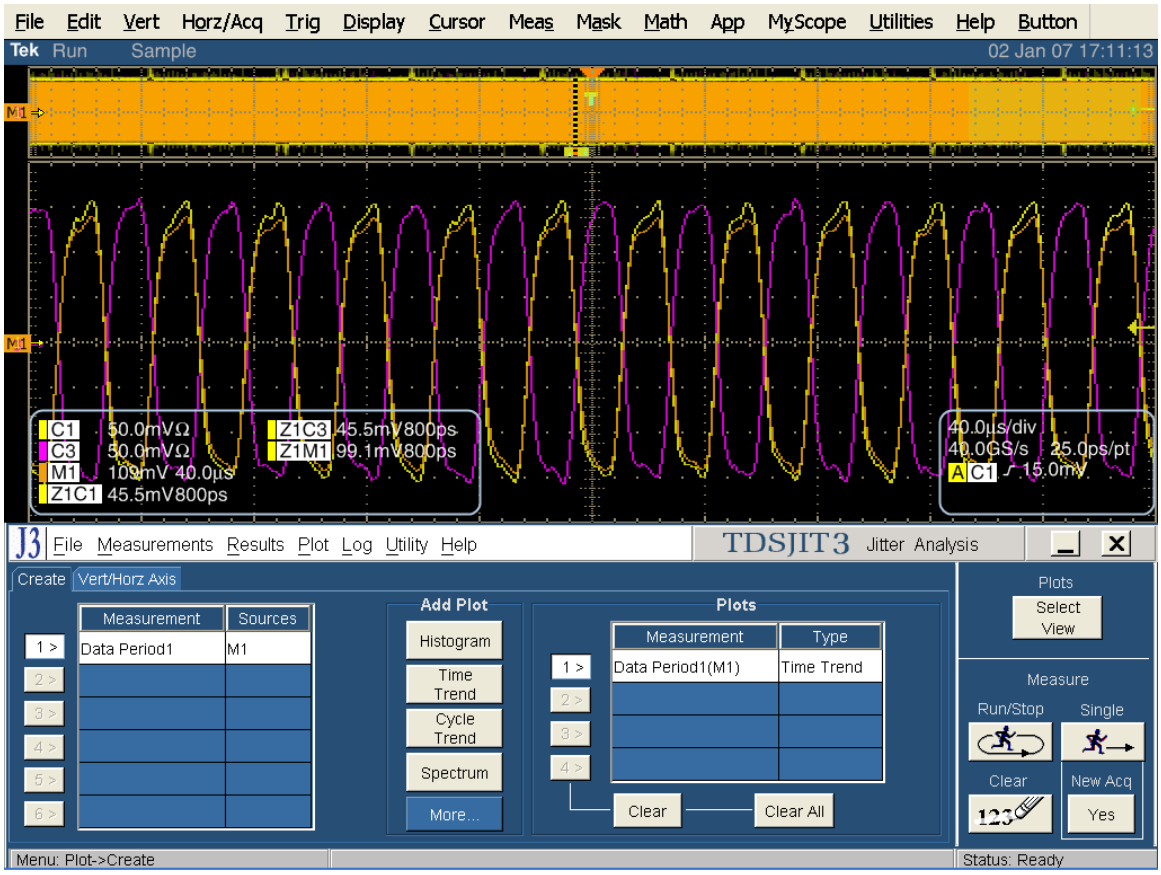
Select Measurement: Data Period on Math1 = Ch1-Ch3.



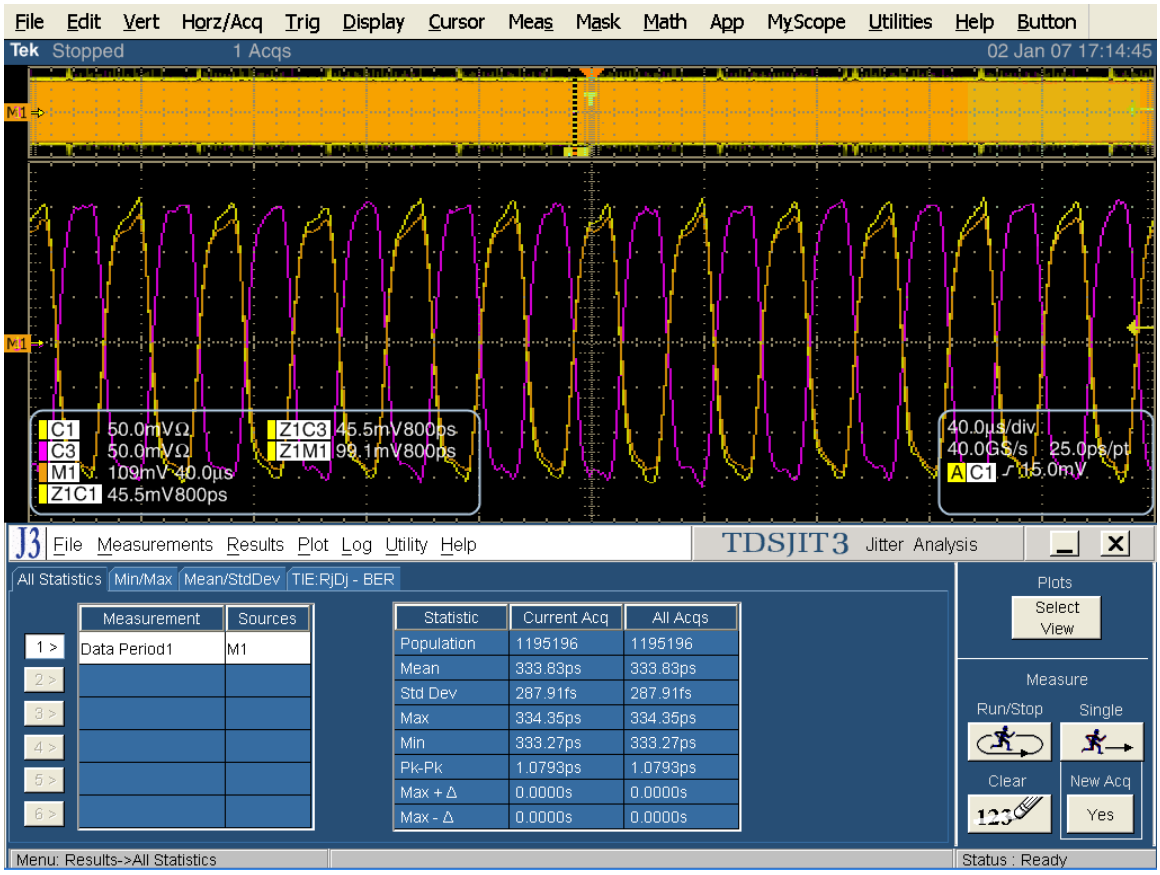
Configure Measurement: Filters Low Pass second order 1.98 MHz.


File Edit Vert Horz/Acq Trig Display Cursor Meas Mask Math App MyScope Utilities Help Button
Tek Run Sample
02 Jan 07 17:09:46
C1 50.0mVΩ
C3 50.0mVΩ
M1 109mV 40.0µs
Z1C1 45.5mV800ps
Z1C3 45.5mV800ps
Z1M1 99.1mV800ps
40.0µs/div
40.0GS/s 25.0ps/pt
A C1 15.0mV
File Measurements Results Plot Log Utility Help
TDSJIT3 Jitter Analysis
Meas Setup Sequence
Select Meas
Configure Meas
Configure Sources
Go to Results
Measurement
Sources
Data Period1
M1
General
Clock Recovery
Filters
F1
F2
Freq
High Pass (F1)
Filter Spec
No Filter
Freq (F1)
1kHz
Low Pass (F2)
Filter Spec
2nd Order
Freq (F2)
1.98MHz
Advanced
Menu: Measurement->Select
Status: Ready

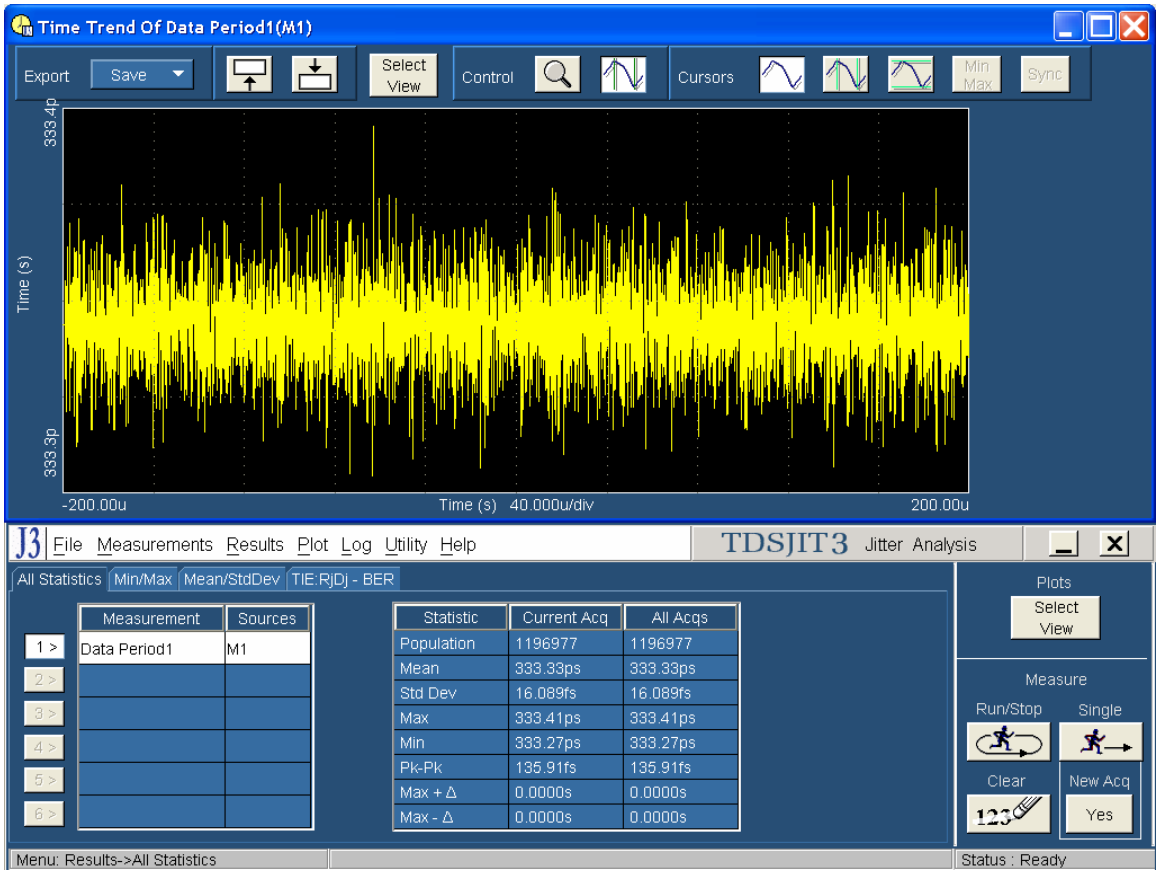
Go to Plot, Create Time Trend for Data Period.



Click on Single to run the application. When complete, the statistics table will contain the results.



For non-SSC PUTs, the period profile is similar to what is shown below:



For the non-SSC measurement, the Mean value in the “Current Acq” column of the Statistics table represents the performance, however again the resolution is not adequate for inspection against the 350 PPM spec.

Use the same procedure to transfer the profile into the scope’s Ref memory, as described above in the SSC measurement to access full measurement resolution.

Calculate deviation = (Nominal – Measured Mean Period)/Nominal * 1e6 ppm

where Nominal is 666.6667 ps for Gen1 PUTs and 333.3333 ps for Gen2 PUTs.

Test PHY-03 - Spread-Spectrum Modulation Frequency

Purpose: To verify that the Spread Spectrum Modulation Frequency of the PUT's transmitter is within the conformance limits.

References:

[1] SATA Standard, 7.2.1, Table 27 – General Specifications
[2] Ibid, 7.2.2.1.5 – Spread-Spectrum Modulation Frequency
[3] Ibid, 7.4.11 – SSC Profile

Resource Requirements:

See appendix A.

Last Template Modification: April 12, 2006 (Version 1.0)

Discussion:

Reference [1] specifies the general PHY conformance limits for SATA PUTs. This specification includes conformance limits for the Spread-Spectrum Modulation Frequency. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

In this test, the Spread-Spectrum Modulation Frequency, f_{SSC}, is measured, based on at least 10 complete SSC cycles.

Test Setup:

Connect equipment as shown in Appendix B, figure 1 or 2 as appropriate. Note that it is acceptable to use either differential or pseudo-differential (single ended plus math waveform) probes for these measurements.

Test Procedure:

Using techniques and equipment as described in Appendix A of the PRE-TEST MOI, or equivalent, place the PUT in BISTFIS mode transmitting an HFTP pattern. Depending on the capability of the PUT, and the equipment available, it is acceptable to use either BIST-T or BIST-L to produce the needed test pattern.

If the PUT supports disconnects, remove the SATA PRE-TEST system, and connect SATA test fixture. Some PUTs require that the connection not be broken after BIST has been activated. In these situations, it may be necessary to use power splitters to allow simultaneous connection of the PRE-TEST system and the test equipment. Refer to Appendix A of the PRE-TEST MOI for additional details.

Start JIT3 application on Scope. Cancel the Jitter Wizard and within JIT3 recall the setup 'SATA SSC and LTF' or 'SATA SSC and LTF Ref Wfm'. See the detailed procedure which follows.

This test is performed once at fastest data rate for the PUT.

Test pattern(s):	**SATA usage model:**
HFTP (SSC ON)	1.5 Gbps and 3Gbps (Gen1i/m and Gen2i/m respectively)

40 us/div (>10 SSC periods), 25 ps/pt

Plot frequency vs time.

Cursor msmt: Record horizontal cursor positions of 10 SSC periods, divide by 10, invert period to SSC modulation frequency.

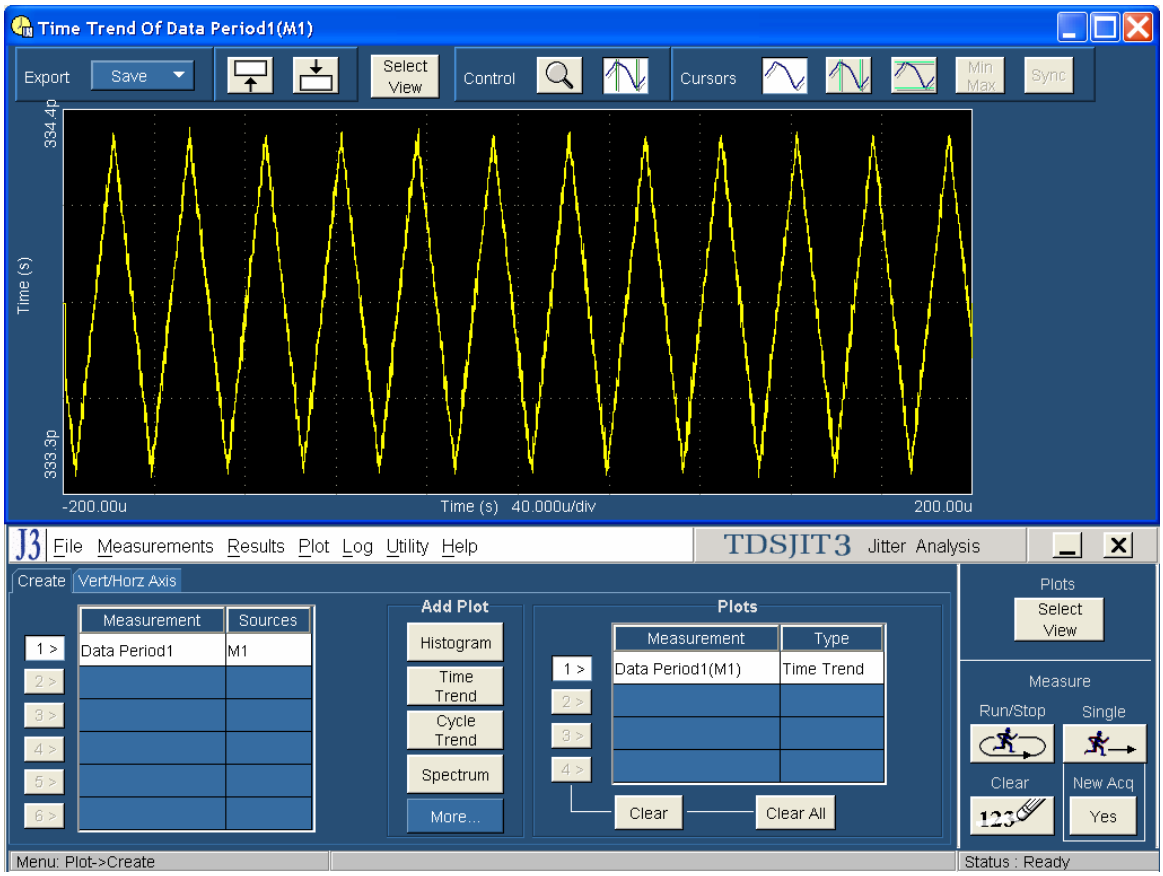
Observable Results:

The Spread-Spectrum Modulation Frequency value shall be between 30 and 33 kHz for both 1.5Gbps and 3.0Gbps PUTs.

Accuracy: +/- 2 ppm

Possible Problems:

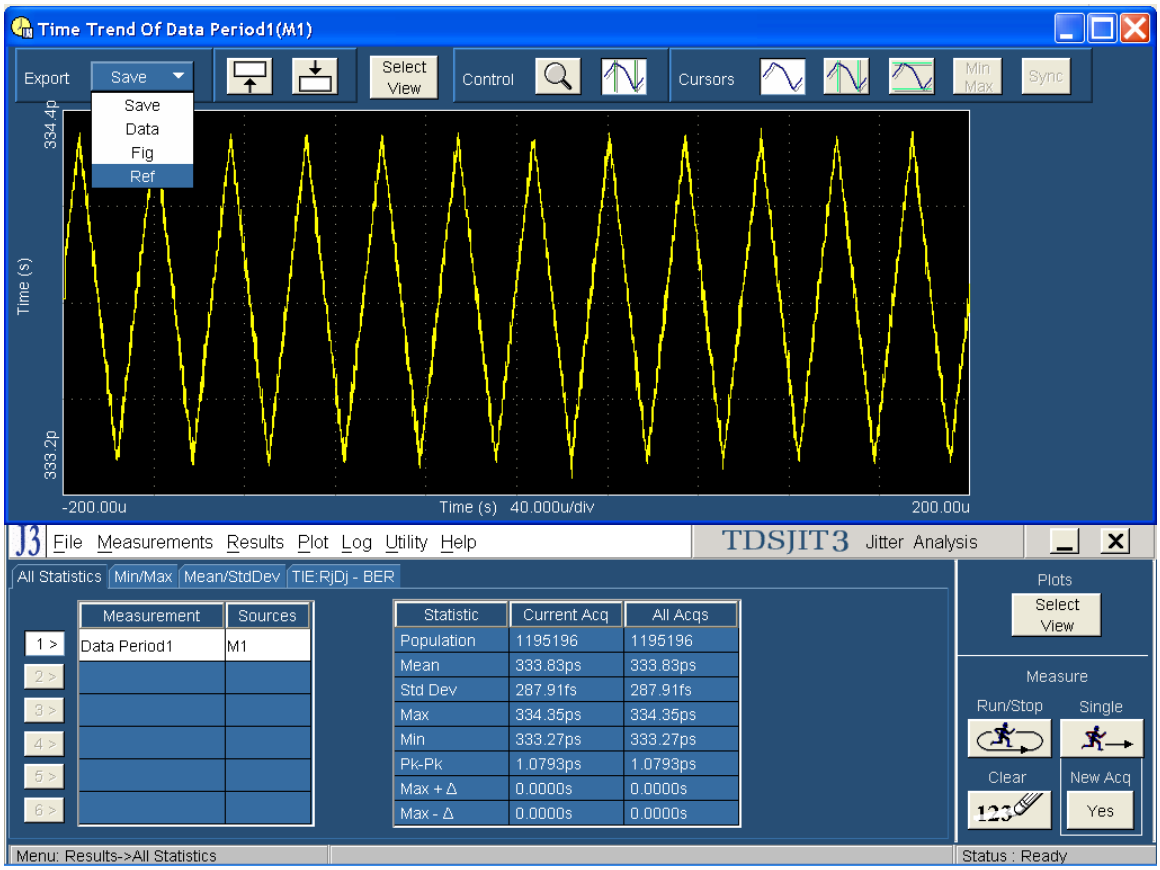
Detailed Procedure:
Follow the procedure described for Phy-02, up to the point where the profile has been created.



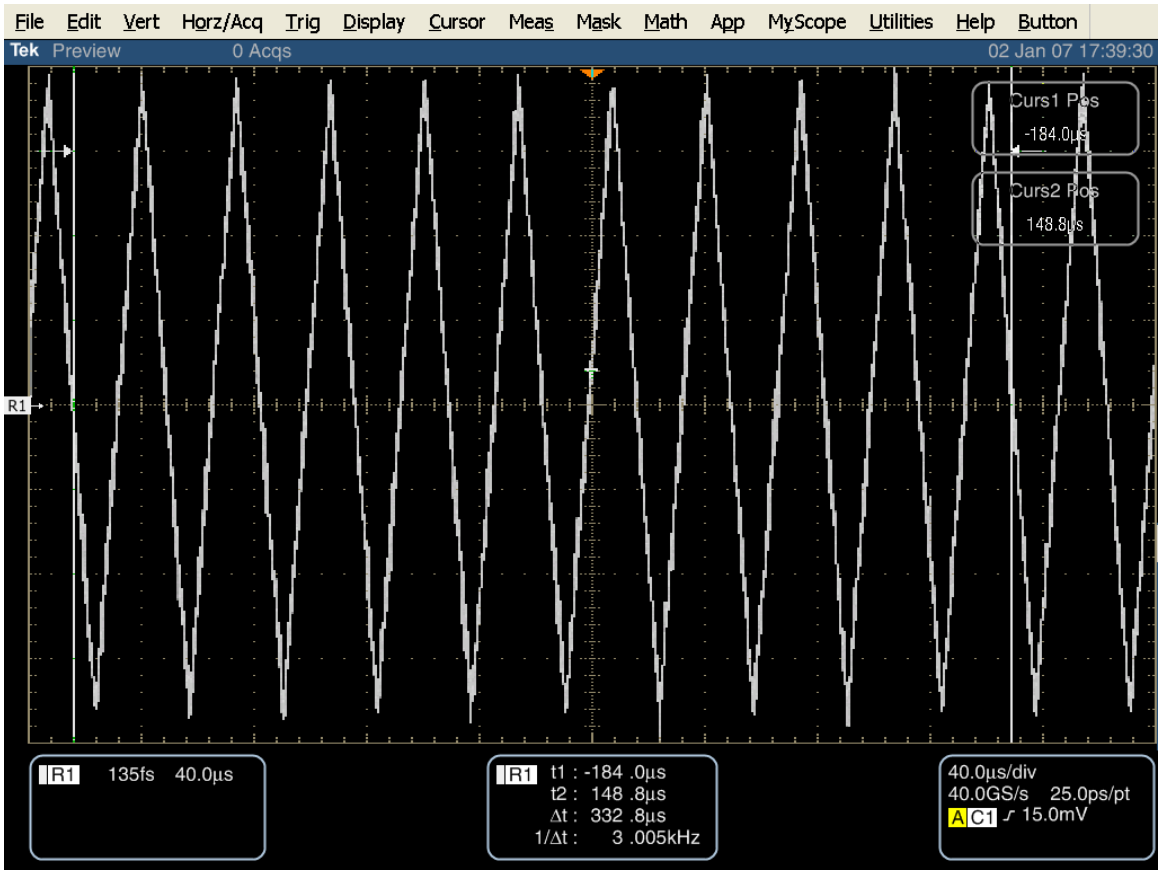
In some cases, it will be adequate to make the measurements using the cursor capability in JIT3 to measure the modulation frequency. Set cursors at the X axis crossing across 10 cycles. To arrive at the modulation frequency, take the delta time value, divide by 10, and invert to get frequency.

Note that there is often substantial higher frequency noise on this profile, and it may be difficult to discern the X axis measurement points on the profile. This is especially critical if the PUT is close to either limit. In this case, it may be preferable to move the waveform into the scope's reference waveform storage, and perform a more critical inspection there. This can be accomplished by using the following process:

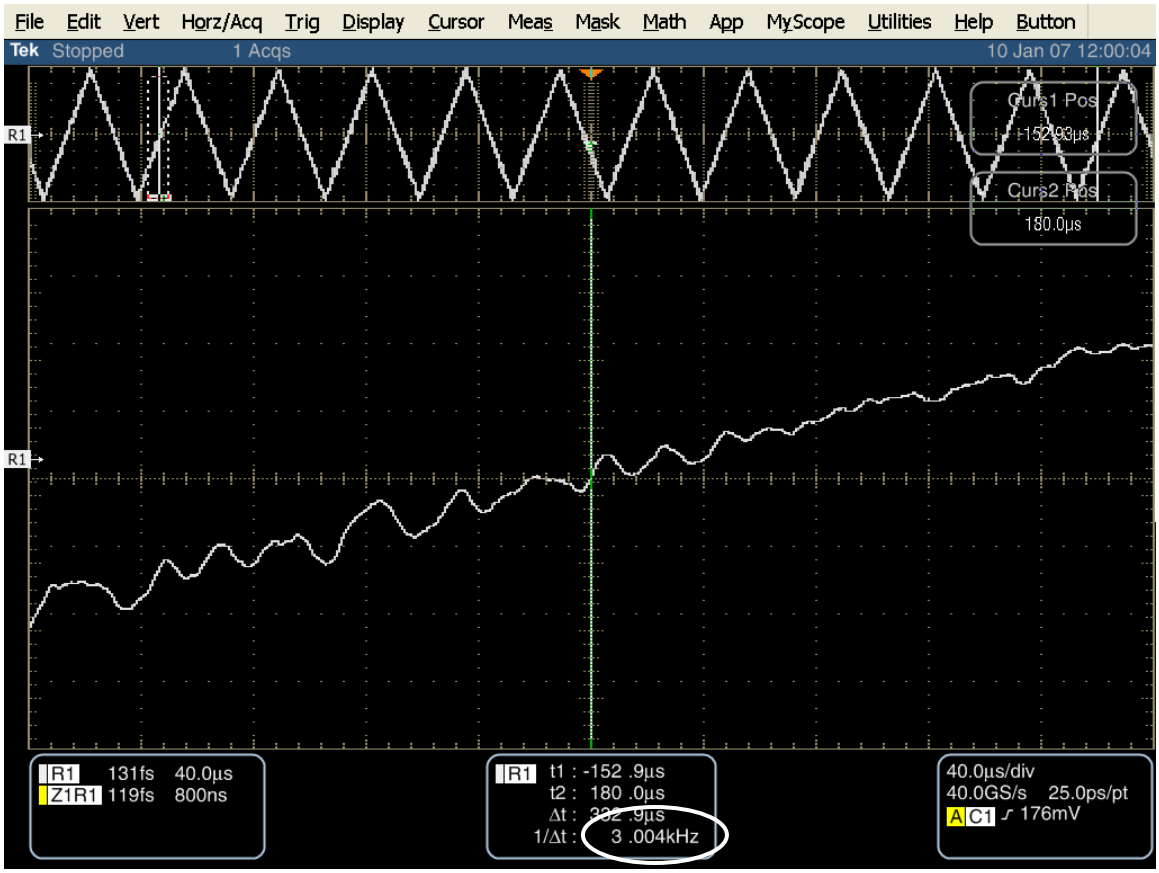
Use the Export: Save function in JIT3's plot screen, and select "Ref" from the pull-down menu.



Once the reference waveform is transferred into the scope's storage, minimize the JIT3 screens, so that only the scope UI is displayed. Turn on the scope cursors, and place across 10 cycles of the profile, as shown.



Using the scope's zoom function, it is possible to more closely inspect the placement of the cursors in making the measurement, as shown in the following image.



Again, it is necessary to divide the period by 10, then invert to get the modulation frequency, or alternatively multiply the 1/Δt value by 10 to get the modulation frequency.

Test PHY-04 - Spread-Spectrum Modulation Deviation

Purpose: To verify that the Spread-Spectrum Modulation Deviation of the PUT's transmitter is within the conformance limits.

References:

[1] SATA Standard, 7.2.1, Table 27 – General Specifications
[2] Ibid, 7.2.2.1.6 – Spread-Spectrum Modulation Deviation
[3] Ibid, 7.4.11 – SSC Profile
[4] SATA unified test document, 2.10.4

Resource Requirements:

See appendix A.

Last Template Modification: April 12, 2006 (Version 1.0)

Discussion:

Reference [1] specifies the general PHY conformance limits for SATA PUTs. This specification includes conformance limits for the Spread-Spectrum Modulation Deviation. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

In this test, the Spread-Spectrum Modulation Deviation is measured, based on at least 10 complete SSC cycles.

Test Setup:

Connect equipment as shown in Appendix B, figure 1 or 2 as appropriate. Note that it is acceptable to use either differential or pseudo-differential (single ended plus math waveform) probes for these measurements.

Test Procedure:

Using techniques and equipment as described in Appendix A of the PRE-TEST MOI, or equivalent, place the PUT in BISTFIS mode transmitting an HFTP pattern. Depending on the capability of the PUT, and the equipment available, it is acceptable to use either BIST-T or BIST-L to produce the needed test pattern.

If the PUT supports disconnects, remove the SATA PRE-TEST system, and connect SATA test fixture. Some PUTs require that the connection not be broken after BIST has been activated. In these situations, it may be necessary to use power splitters to allow simultaneous connection of the PRE-TEST system and the test equipment. Refer to Appendix A of the PRE-TEST MOI for additional details.

Start JIT3 application on Scope. Cancel the Jitter Wizard and within JIT3 recall the setup 'SATA SSC and LTF' or 'SATA SSC and LTF Ref Wfm'. Follow the same procedure as described for Phy-02, except that for the final result, the "Max" is read and compared against the limits.

This test is performed once at fastest data rate for the PUT.

Test pattern(s):	**SATA usage model:**
HFTP (SSC ON)	1.5 Gbps and 3Gbps (Gen1i/m and Gen2i/m respectively)

40 us/div (>10 SSC periods), 25 ps/pt

Record min, max frequency from results overview.
Calculate deviation=(Nominal – Measured Mean Max Period)/Nominal * 1e6 ppm.

No greater than -5350 (+350 to -5350) assuming (Nominal – Measured Mean Max Period)/Nominal * 1e6 ppm

Observable Results:

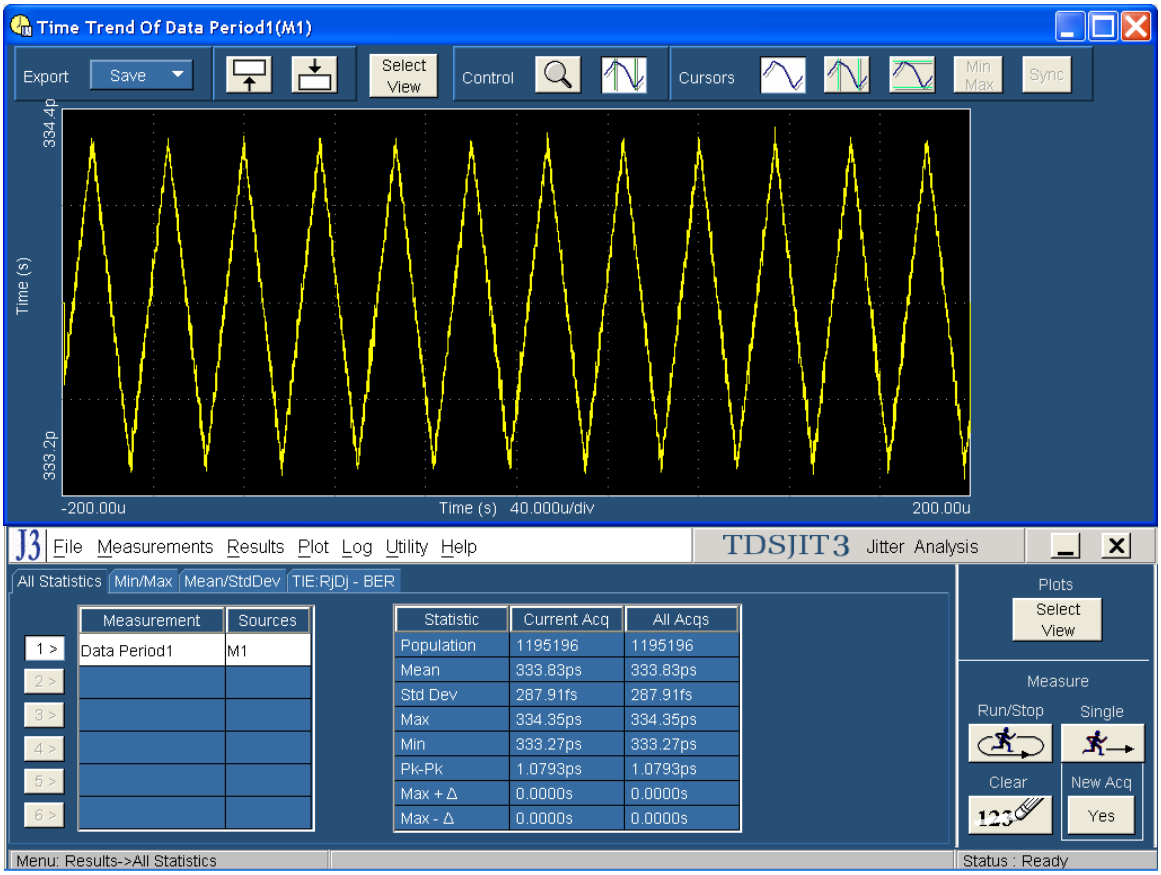
The Spread-Spectrum Modulation Deviation value shall be between –5350 and +350 ppm for both 1.5Gbps and 3.0Gbps PUTs.

Accuracy: +/- 2 ppm

Possible Problems:

Detailed Procedure:

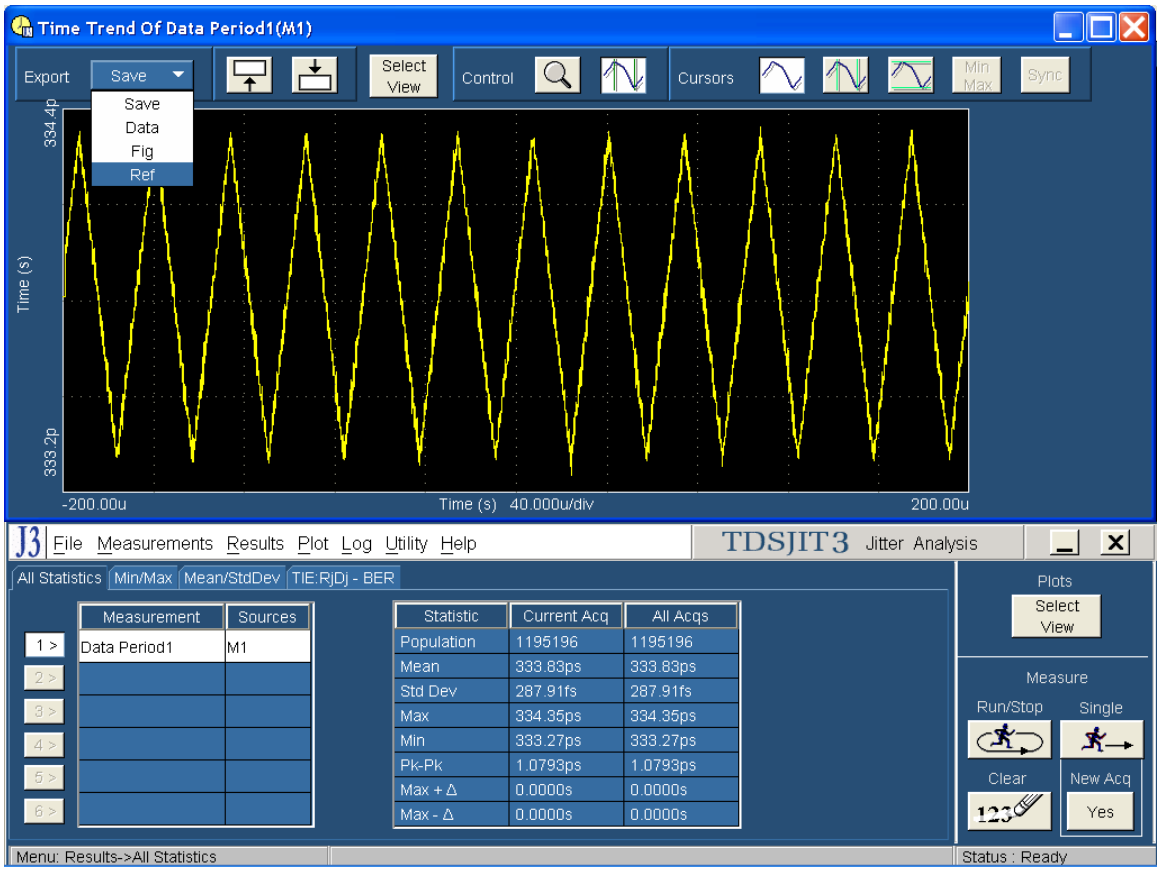
Follow the same procedure as described for Phy-02 up to the point where the profile is generated. The SSC profile will be similar to what is shown below:



NOTE: The TDSJIT3 software provides the ability to do cursor measurements directly on the profile plot. However, the 4 digits of resolution obtained when using JIT3 cursor measurements (1000 ppm) is not sufficient for this test.

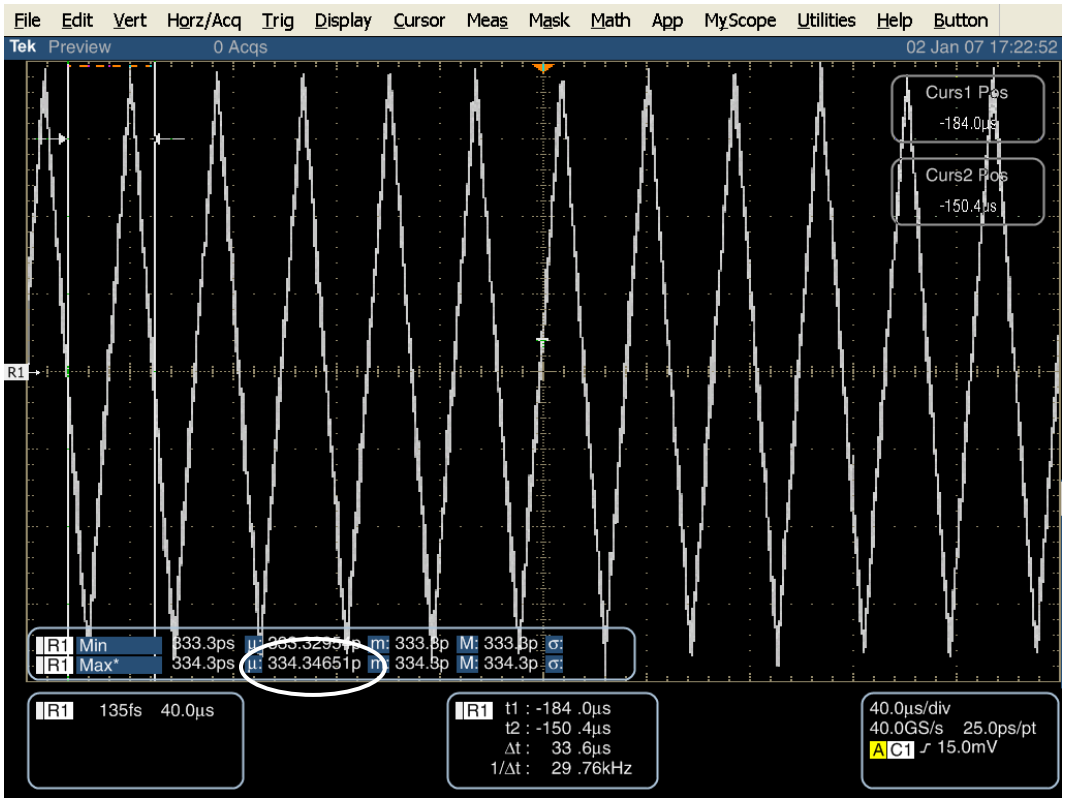
The value can also be read directly from the statistics table as seen in the previous figure. This data is shown as 5 digits, and provides a 100 ppm resolution, which is marginally adequate for the measurement tolerance. For Phy-04, use the Max value shown in the "Current Acq" column.

To get 8 digits of resolution, use the Export: Save function in JIT3's plot screen, and select "Ref" from the pull-down menu. This transfers the Frequency Profile into the scope's Ref waveform memory. See the procedure in Phy-02 for more details. Enable Amplitude Min measurement, and read the Mean (μ) in the measurement frame.



Record each of 10 max period peak points. Average these values to determine the Measured Mean Max period.

Record each of 10 min period peak points. Average these values to determine the Measured Mean Min period.



Calculate deviation = (Nominal – Measured Mean Max)/Nominal * 1e6 ppm

Calculate deviation = (Nominal – Measured Mean Min Period)/Nominal * 1e6 ppm,

where Nominal is 666.6667 ps for Gen1 PUTs and 333.3333 ps for Gen2 PUTs.

PHY TRANSMITTED SIGNAL REQUIREMENTS (TSG 1-12)

Overview:

This group of tests verifies the Phy Transmitted Signal Requirements, as defined in Section 2.14 of the SATA Interoperability Unified Test Document, v1.3 (which references the SATA Standard, v2.6).

Test TSG-01 - Differential Output Voltage

Purpose: To verify that the Differential Output Voltage of the PUT's transmitter is within the conformance limits.

References:

[1] SATA Standard, 7.2.1, Table 29 – Transmitted Signal Requirements
[2] Ibid, 7.2.2.3.1 – TX Differential Output Voltage
[3] Ibid, 7.4.4 – Transmitter Amplitude
[4] SATA unified test document, 2.12.1

Resource Requirements:

See appendix A

Last Template Modification: May 15, 2006 (Version 1.0)

Discussion:

Reference [1] specifies the Transmitted Signal conformance limits for SATA PUTs. This specification includes conformance limits for the Differential Output Voltage. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

Test Setup:

Connect equipment as shown in Appendix B, figure 1 or 2 as appropriate. Note that it is acceptable to use either differential or pseudo-differential (single ended plus math waveform) probes for these measurements.

Test Procedure:

Using techniques and equipment as described in Appendix A of the PRE-TEST MOI, or equivalent, place the PUT in BISTFIS mode transmitting an HFTP pattern. Depending on the capability of the PUT, and the equipment available, it is acceptable to use either BIST-T or BIST-L to produce the needed test pattern.

If the PUT supports disconnects, remove the SATA PRE-TEST system, and connect SATA test fixture. Some PUTs require that the connection not be broken after BIST has been activated. In these situations, it may be necessary to use power splitters to allow simultaneous connection of the PRE-TEST system and the test equipment. Refer to Appendix A of the PRE-TEST MOI for additional details.

Start RT-Eye application on Scope. Select SATA module under "Modules" menu item. Select Differential Voltage from Amplitude Measurement. See the following detailed procedure for additional information.

RT-Eye software will prompt for each test pattern as it is required. Repeat the PRE-TEST process described above for each of the required test patterns. Testing with SSC is optional.

Test pattern(s):	**SATA usage model:**
HFTP, MFTP, and LFTP, and LBP or HFTP, MFTP, and LFTP (SSC optional)	1.5 Gbps and 3Gbps (Gen1i/m and Gen2i/m respectively)

Gen1: 10 us/div, 50 ps/pt (> 100,000 UI)
Gen2: 4 us/div, 25 ps/pt (> 100,000 UI)

Observable Results:

For the interests of the Interoperability Program, the measurements will only be taken to verify this requirement at the minimum limit of 400mV. Within the specification, there are two options for measuring the minimum:

- Vtest = min(DH, DM, VtestLBP)
- Vtest = min(DH, DM, VtestAPP)

Note that gathering a minimum result from either of the options above is acceptable. It is not required to report a result for both.

In the interest of ensuring products meet some metric for system interoperability at the maximum limit, the maximum value received out of the minimum measurement will be verified to not exceed 800mV using the formulas below, where DH, DM, VtestLBP, and VtestAPP are the same values used for the above minimum measurement.

- Vtest(max) = max(DH, DM, VtestLBP)
- Vtest(max) = max(DH, DM, VtestAPP)

Accuracy: 0.5 % rms

Possible Problems:
Per ECN-18, a new LBP pattern was defined that eliminates the disparity ambiguity, as described below. Use ECN-18 compliant LBP for performing the amplitude test whenever possible.

If an ECN-18 LBP is not available, it is possible to use the older LBP pattern. However, a pattern mismatch error can occur. To avoid the pattern mismatch problem, make sure that the real lone bit pattern with positive disparity is used (0011 0110 1111 0100 0010 0011 0110 1111 0100 0010 0011 0110 etc….).
This pattern has a lone '1' bit between 4 '0's and 3 '0's, and is required for the algorithm. Visually verify the proper disparity on LBP by zooming in on the acquired waveform, and inspecting the waveform for a section that contains a "00001000" section. If this pattern is not readily apparent, re-load the LBP BISTFIS pattern into the PUT, and reacquire the waveform, then repeat the inspection until the proper pattern is seen. Once the proper pattern is detected, continue running the test. It is only necessary to make this inspection on LBP patterns, as there is a 50% chance of getting the desired positive disparity each time the LBP is loaded into the PUT.

Detailed Procedure:

Start RT-Eye application on Scope. Select SATA module under "Modules" menu item. Select Differential Voltage from Amplitude Measurement.

Select correct probe type.

Press configure.

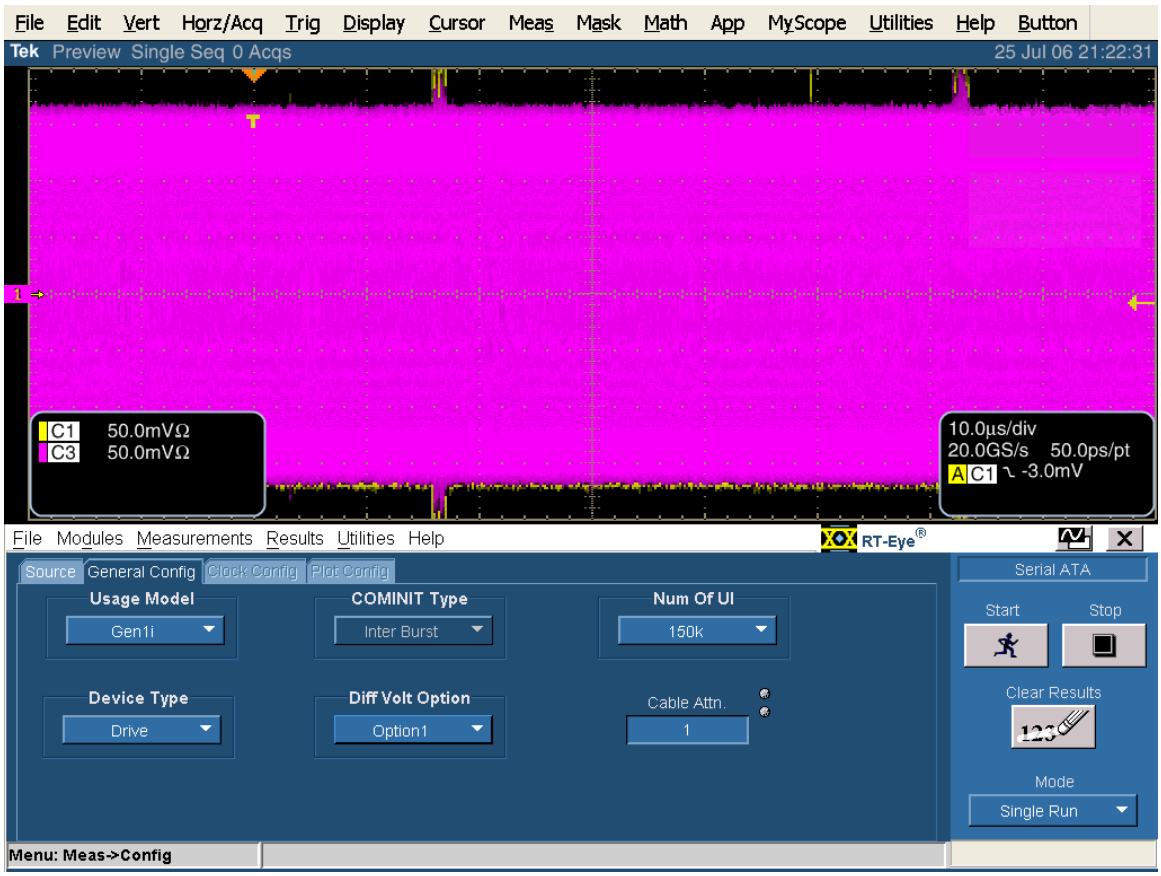
Source configuration (Source tab):

Select BIST FIS/User Test Method. Select correct Source Type and channels.

General configuration (General Config tab):

Select correct Usage Model, Device Type, Diff Volt Option Option2, and Number of UI 150k.

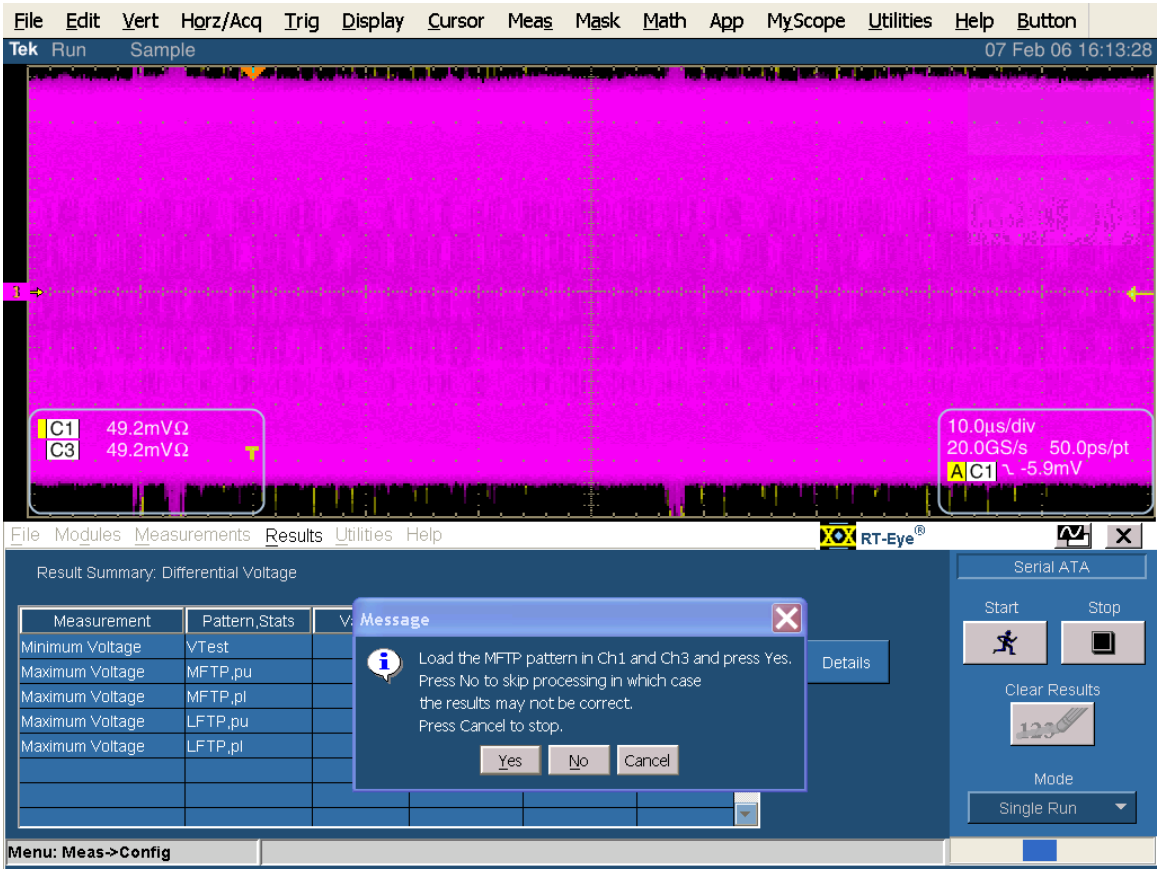
Press Start


File Edit Vert Horz/Acq Trig Display Cursor Meas Mask Math App MyScope Utilities Help Button
Tek Preview Single Seq 0 Acqs
25 Jul 06 21:22:31
C1 50.0mVΩ
C3 50.0mVΩ
10.0µs/div
20.0GS/s 50.0ps/pt
A C1 -3.0mV
File Modules Measurements Results Utilities Help
RT-Eye®
Source General Config Clock Config Plot Config
Usage Model
Gen1i
COMINIT Type
Inter Burst
Num Of UI
150k
Device Type
Drive
Diff Volt Option
Option1
Cable Attn.
1
Serial ATA
Start
Stop
Clear Results
Mode
Single Run
Menu: Meas->Config

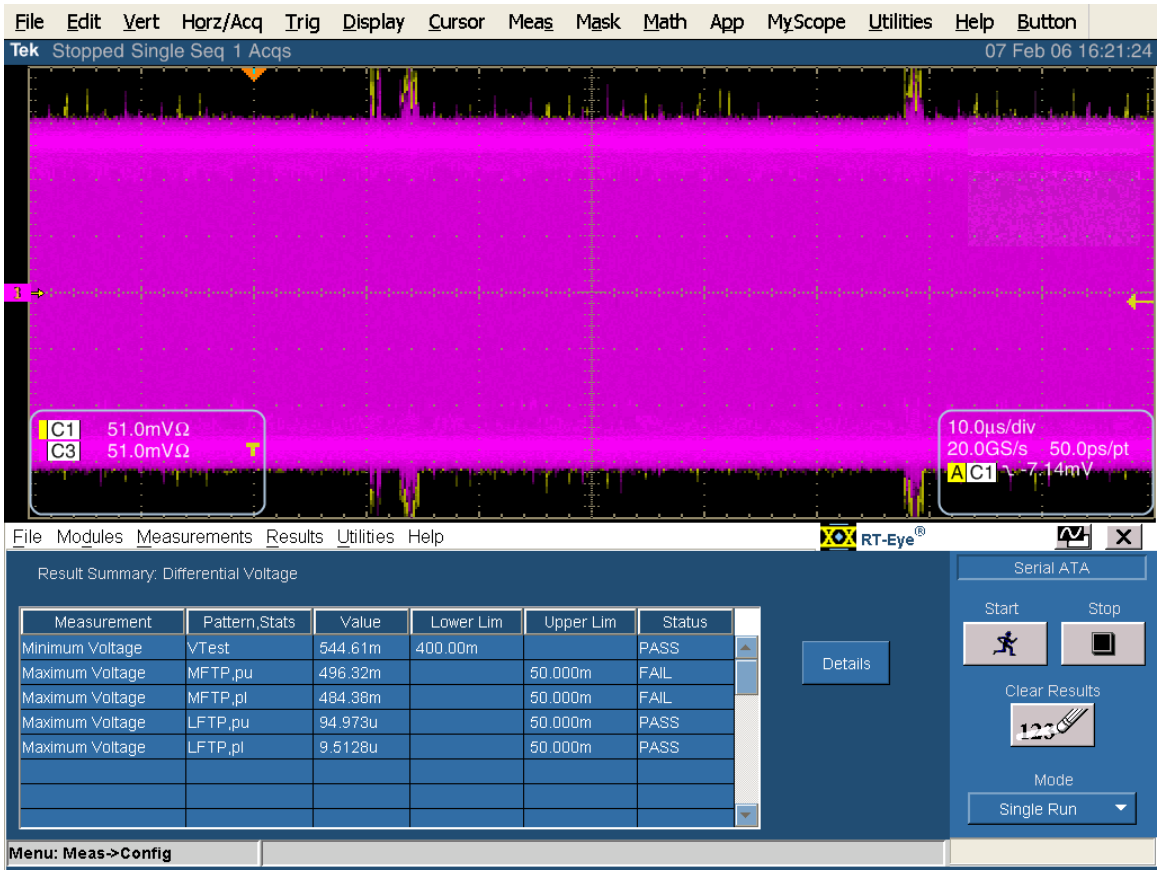
The software will prompt for the HFTP test pattern. Use BIST FIS to initiate HFTP from the PUT or load the correct waveform files. Press Yes.

The software will next prompt for the MFTP test pattern. Use BIST FIS to initiate MFTP from the PUT or load the correct waveform files. Press Yes.

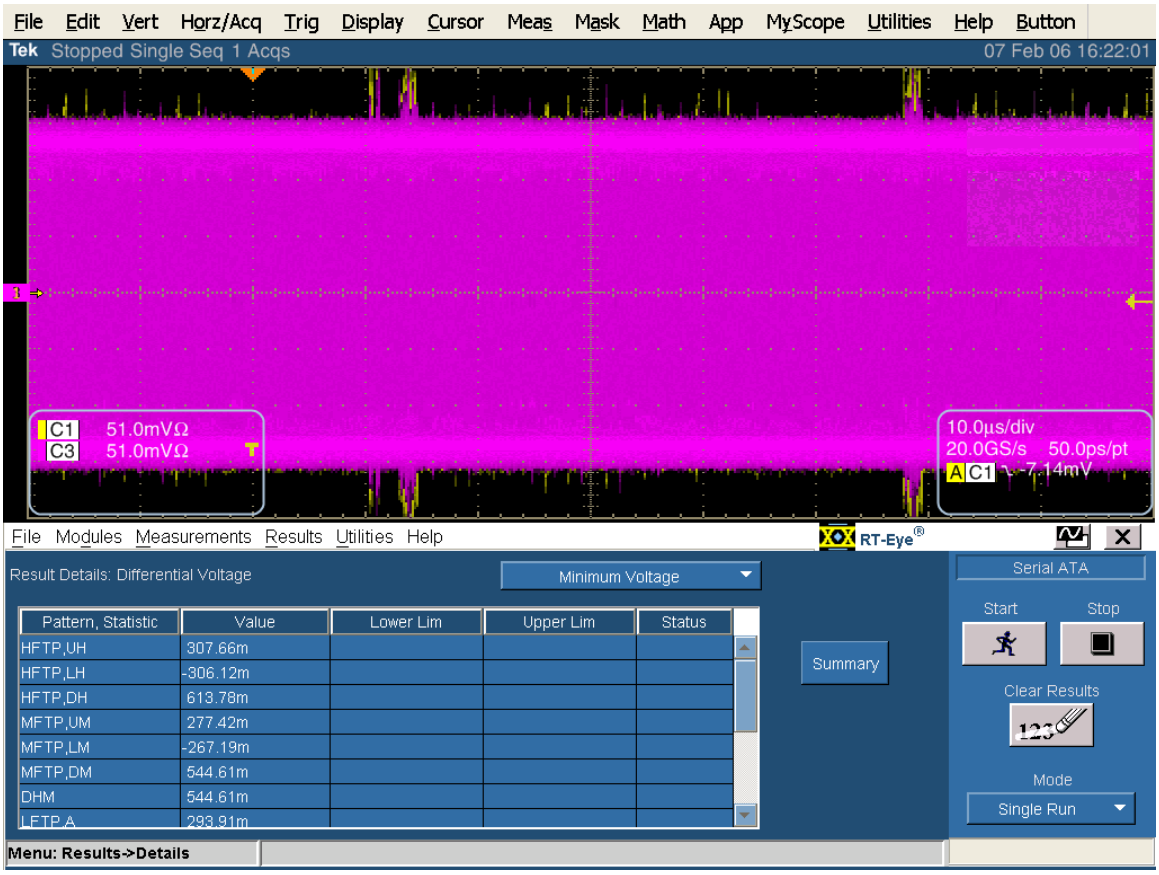
The software will next prompt for the LFTP test pattern. Use BIST FIS to initiate LFTP from the PUT or load the correct waveform files. Press Yes.



View results in Results Summary.



View additional results in Details.



Vtest(min) must be >= 400mV.

New procedure for maximum differential output voltage

To calculate the maximum differential output voltage, go to the details of minimum voltage (see above) and determined one of the following maxima:

- Vtest(max) = max(DH, DM, VtestLBP)
- Vtest(max) = max(DH, DM, VtestAPP)

The maximum value calculated cannot exceed 800mV.

Test TSG-02 - Rise/Fall Time

Purpose: To verify that the Rise/Fall time of the PUT's transmitter is within the conformance limits.

References:

[1] SATA Standard, 7.2.1, Table 29 – Transmitted Signal Requirements
[2] Ibid, 7.2.2.3.3 – TX Rise/Fall Time
[3] Ibid, 7.4.3 – Rise and Fall Times
[4] SATA unified test document, 2.12.2

Resource Requirements:

See appendix A.

Last Template Modification: May 15, 2006 (Version 1.0)

Discussion:

Reference [1] specifies the Transmitted Signal conformance limits for SATA PUTs. This specification includes conformance limits for the Rise/Fall Time. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

Test Setup:

Connect equipment as shown in Appendix B, figure 1 or 2 as appropriate. Note that it is acceptable to use either differential or pseudo-differential (single ended plus math waveform) probes for these measurements.

Test Procedure:

Using techniques and equipment as described in Appendix A of the PRE-TEST MOI, or equivalent, place the PUT in BISTFIS mode transmitting an HFTP pattern. Depending on the capability of the PUT, and the equipment available, it is acceptable to use either BIST-T or BIST-L to produce the needed test pattern.

If the PUT supports disconnects, remove the SATA PRE-TEST system, and connect SATA test fixture. Some PUTs require that the connection not be broken after BIST has been activated. In these situations, it may be necessary to use power splitters to allow simultaneous connection of the PRE-TEST system and the test equipment. Refer to Appendix A of the PRE-TEST MOI for additional details.

Start JIT3 application on Scope. Recall the setup: 'SATA UI rise fall wfm gen1' or 'SATA UI rise fall wfm gen2', depending on the data rate being tested. If using reference waveforms, recall the setup 'SATA UI rise fall ref wfm gen1' or 'SATA UI rise fall ref wfm gen2'. See the following detailed procedure for additional information.

Repeat for all specified test patterns and data rates. Testing with SSC is optional.

Test pattern(s):	**SATA usage model:**
HFTP (SSC optional)	1.5 Gbps and 3Gbps (Gen1i/m and Gen2i/m respectively)

Gen1: 10 us/div, 50 ps/pt (> 100,000 UI)
Gen2: 4 us/div, 25 ps/pt (> 100,000 UI)

Observable Results:

The TX Rise/Fall Times shall be between the limits specified in reference [1]. For convenience, the values are reproduced below.

Note: Failures at minimum rate have not been shown to affect interoperability and will not be included in determining pass/fail for Interop testing

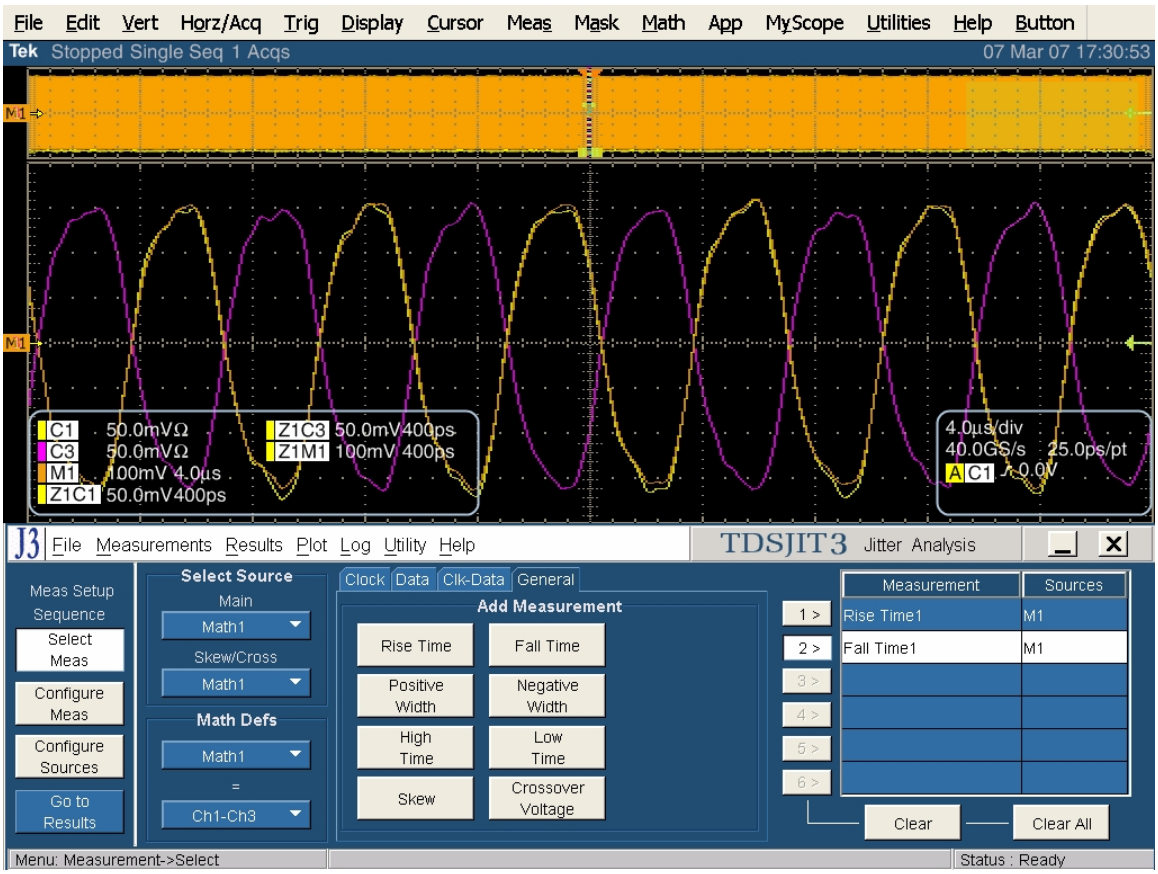
PUT Type	RFT Min	RFT Max
Gen1i and Gen1m	100 ps	273 ps
Gen2i and Gen2m	67 ps	136 ps

Accuracy: 1.6 % typical gen2

Possible Problems:

Detailed Procedure:

Start JIT3 application on Scope. Select Source Main as “Math1”, and define Math1 as pseudo-differential (e.g. CH1-CH3). Select General tab, and add measurement for Rise Time and Fall Time.



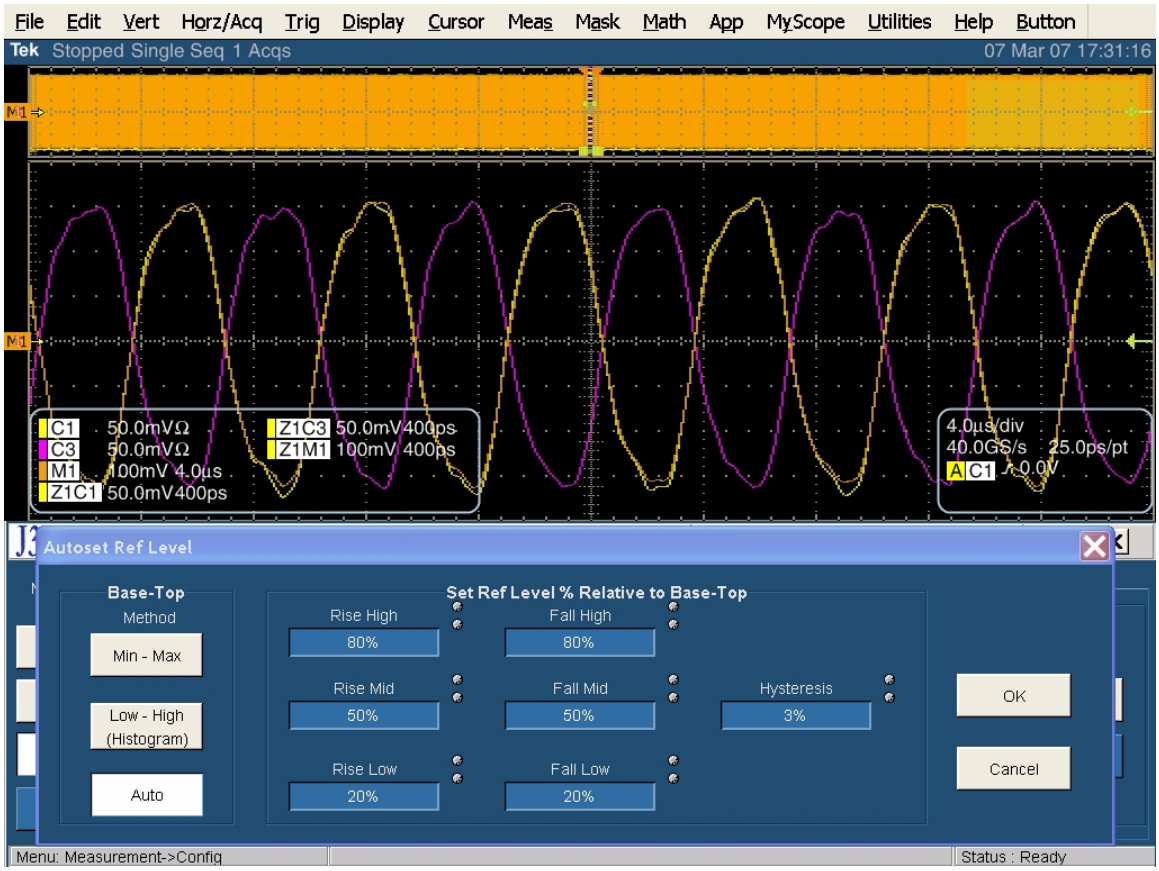
Click on the “Configure Sources” button in the “Meas Setup Sequence” frame.

Click on the “Ref Levels” tab.

Click “Setup” in the “Autoset” frame.

Set the Rise High and Fall High to 80%

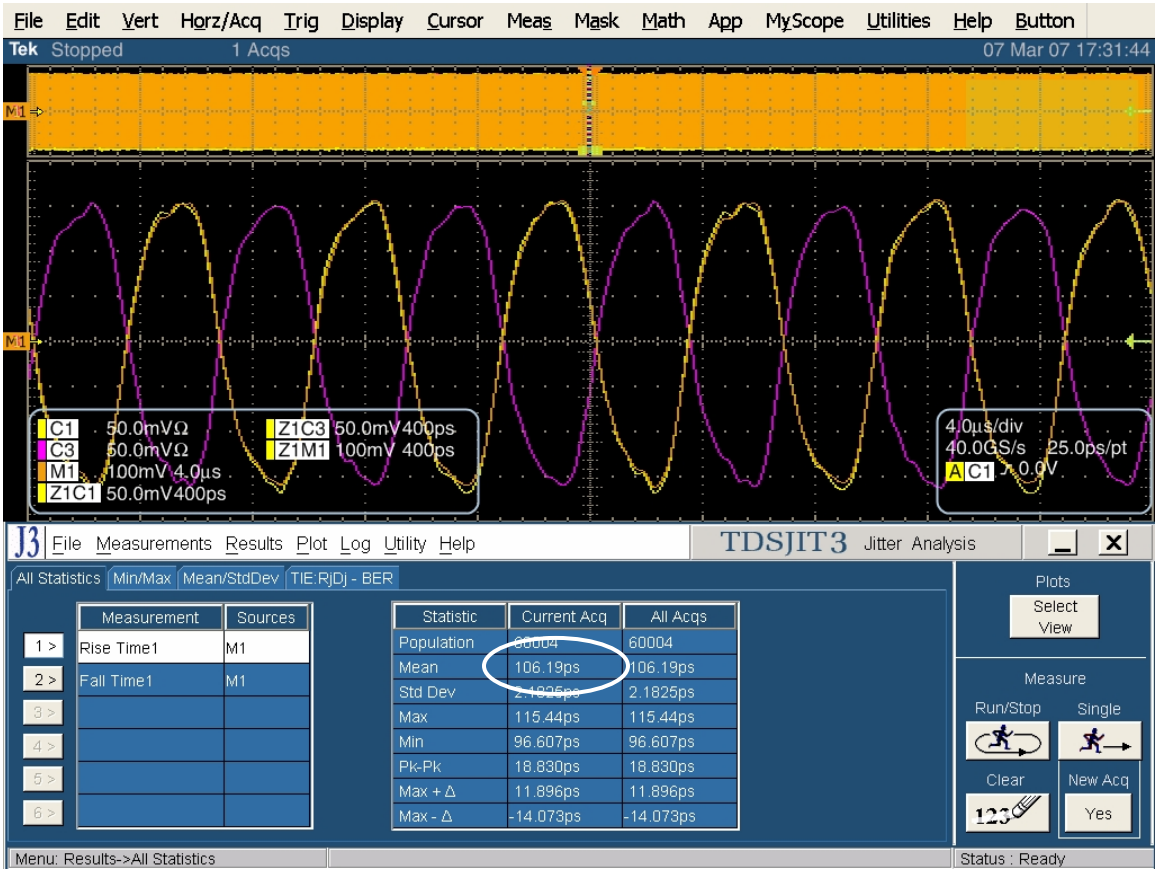
Set the Rise Low and Fall Low to 20%



When finished, click on “OK”.

Click on “Go to Results” in “Meas Setup Sequence” frame.

Click on “Single” to run analysis. The following screen capture shows typical results:

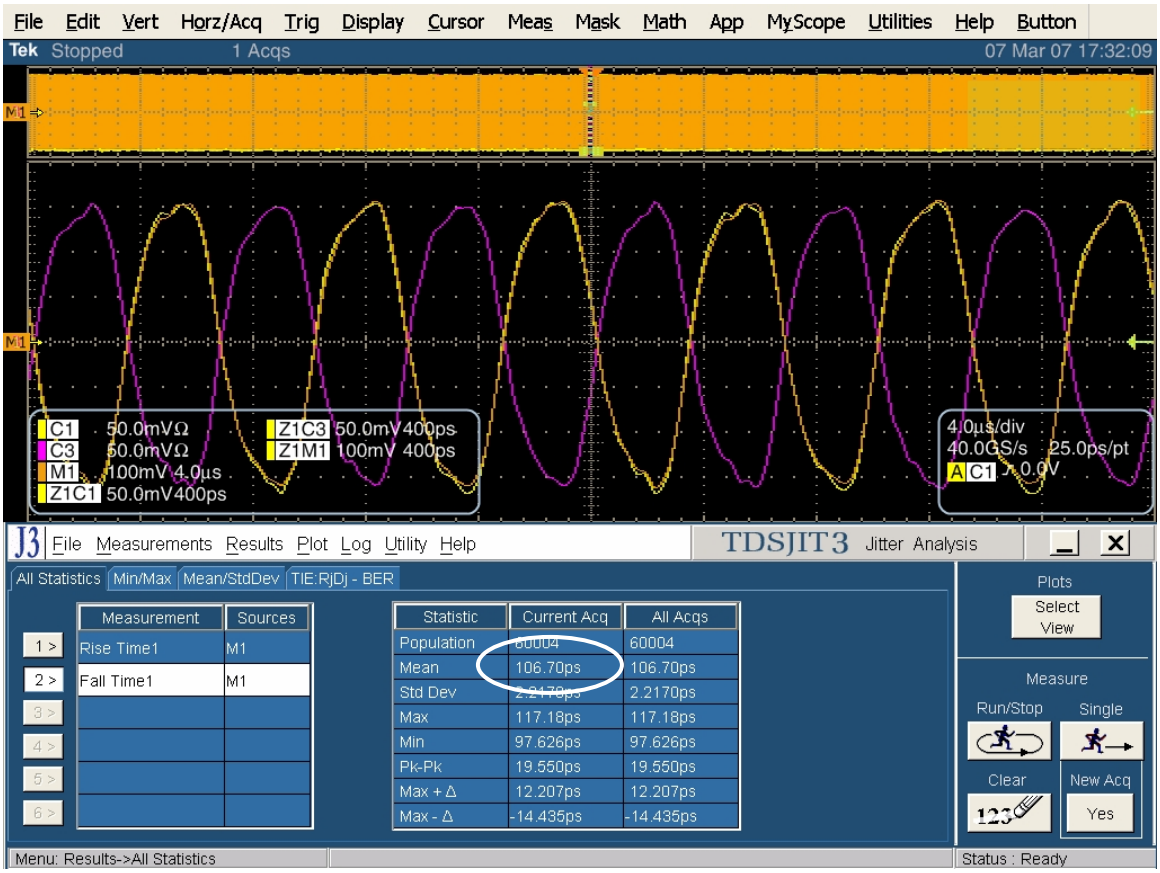


Compare the Mean value from the Current Acq column in the results screen against the limits allowed by the specification.

Gen1 PUTs must be between 100ps and 273ps, while Gen2 PUTs must be between 67ps and 136ps.

PUTs demonstrating rise times at or below minimum rate have not been shown to affect interoperability and will not be included in determining pass/fail for Interop testing

Click on “Fall Time” in the measurement table, and statistics will be displayed for the fall time analysis.



Compare the Mean value from the Current Acq column in the results screen against the limits allowed by the specification.

Gen1 PUTs must be between 100ps and 273ps, while Gen2 PUTs must be between 67ps and 136ps.

PUTs demonstrating rise times at or below minimum rate have not been shown to affect interoperability and will not be included in determining pass/fail for Interop testing

Test TSG-03 - Differential Skew

Purpose: To verify that the Differential Skew of the PUT's transmitter is within the conformance limits.

References:

[1] SATA Standard, 7.2.1, Table 29 – Transmitted Signal Requirements
[2] Ibid, 7.2.2.3.4 – TX Differential Skew (Gen2i, Gen1x, Gen2x)
[3] Ibid, 7.4.12 – Intra-pair Skew
[4] SATA unified test document, 2.12.3

Resource Requirements:

See appendix A.

Last Template Modification: April 12, 2006 (Version 1.0)

Discussion:

Reference [1] specifies the Transmitted Signal conformance limits for SATA PUTs. This specification includes conformance limits for Differential Skew. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

Test Setup:

Connect equipment as shown in Appendix B, figure 1A or 2A as appropriate. Note that it is only acceptable to use two single ended SMA connections for these measurements.

Test Procedure:

Using techniques and equipment as described in Appendix A of the PRE-TEST MOI, or equivalent, place the PUT in BISTFIS mode transmitting an HFTP pattern. Depending on the capability of the PUT, and the equipment available, it is acceptable to use either BIST-T or BIST-L to produce the needed test pattern.

If the PUT supports disconnects, remove the SATA PRE-TEST system, and connect SATA test fixture. Some PUTs require that the connection not be broken after BIST has been activated. In these situations, it may be necessary to use power splitters to allow simultaneous connection of the PRE-TEST system and the test equipment. Refer to Appendix A of the PRE-TEST MOI for additional details.

Start JIT3 v2 application on Scope. Use the combined setup 'SATA skew_RF imb_amp imb ref wfm'. Take the average of both skew results. See the following detailed procedure for additional information.

Repeat the PRE-TEST procedure described above for each specified test pattern. This test is only done at the fastest data rate of the PUT. Testing with SSC is optional.

Test pattern(s):	**SATA usage model:**
HFTP, MFTP (SSC optional)	1.5 Gbps and 3Gbps (Gen1i/m and Gen2i/m respectively)

Gen1: 10 us/div, 50 ps/pt (> 100,000 UI)
Gen2: 4 us/div, 25 ps/pt (> 100,000 UI)

Observable Results:

The TX Differential Skew shall be between the limits specified in reference [1]. For convenience, the values are reproduced below.

PUT Type	Max Diff Skew
Gen1i and Gen1m	20 ps

Gen2i and Gen2m	20 ps

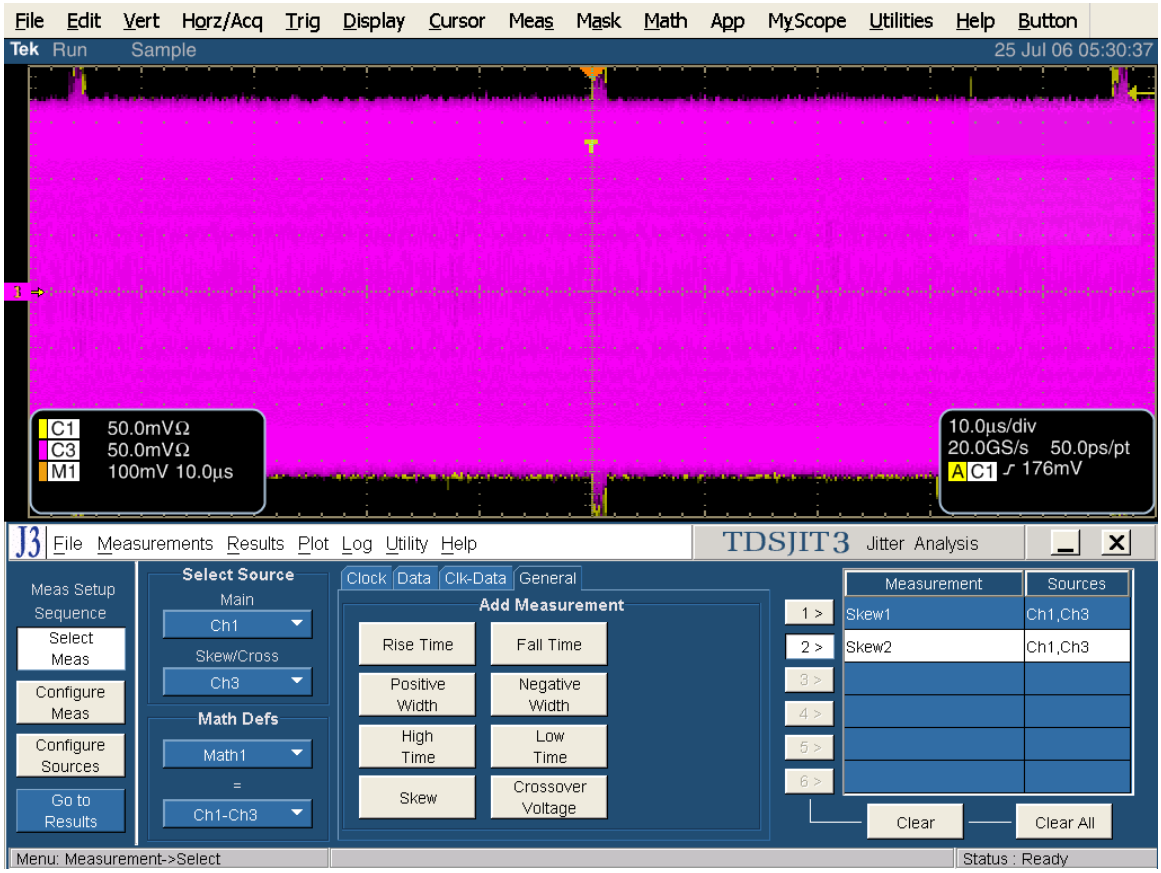
Accuracy: 3 ps rms

Possible Problems:

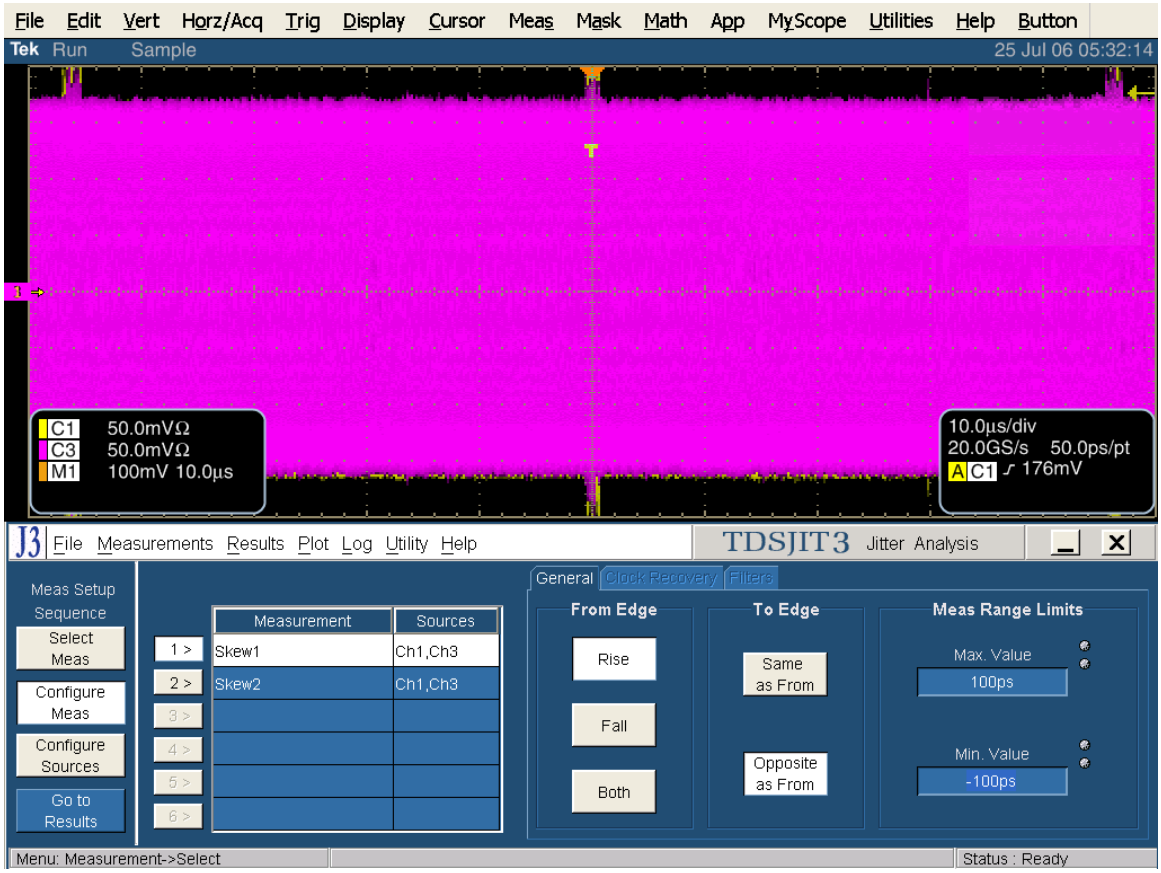
Detailed Procedure:

Run JIT3 version 2 by selecting App, Jitter Analysis – Advanced, from the Oscilloscope menu.

Set Main channel for ch1, and Skew/Cross channel to other channel used for pseudo-differential connection (Ch3 in this example). Select 2 skew measurements (click on “Skew” two times) from the general tab.

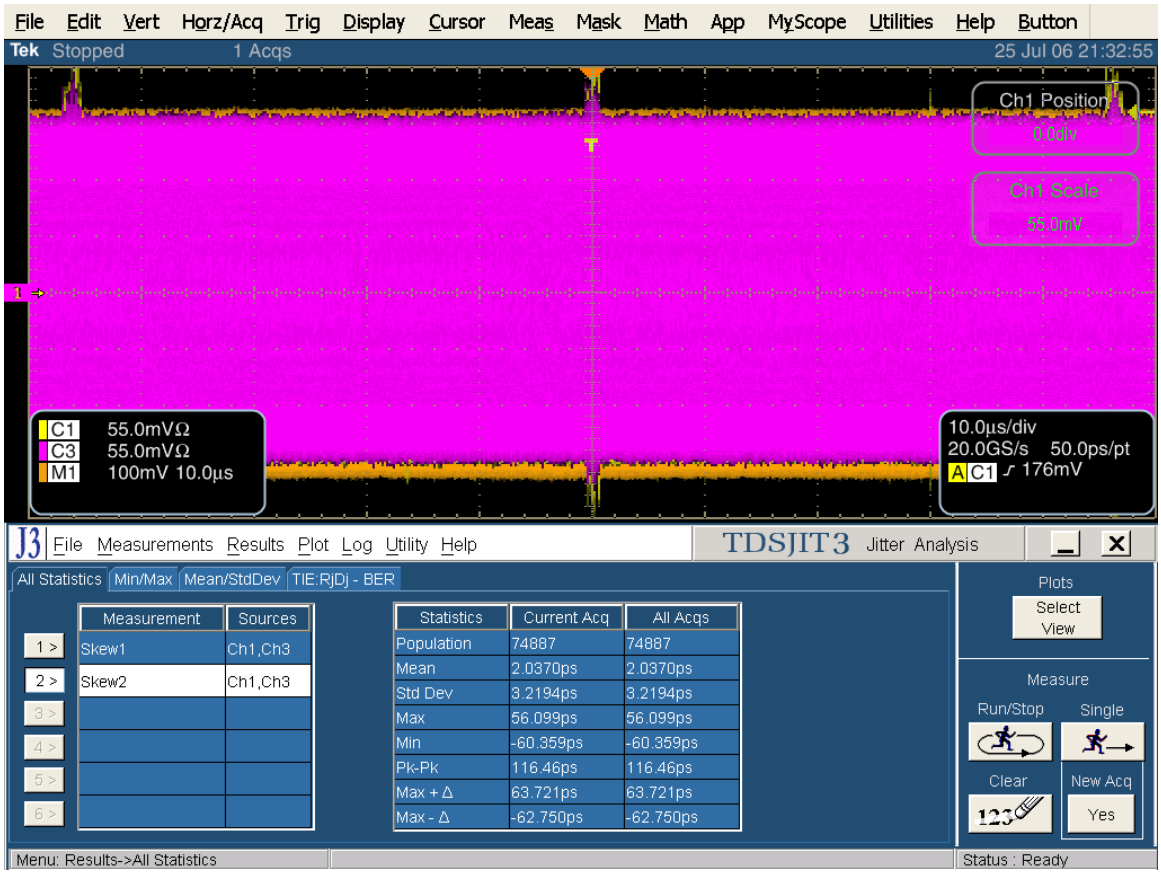


Click on the Configure Meas button. Highlight Skew1 by clicking on the "1>" button next to it. Configure Skew1 from rising edge to opposite edge, with +/-100 ps measurement range limits. This sets up the first part of the measurement from rising edge of channel 1 to the falling edge of channel 3. This is shown in the lower portion of the following diagram:



Highlight Skew2 by clicking on the “2>” button next to it. Configure Skew2 from falling edge to opposite edge, with +/-100 ps measurement range limits. This sets up the second part of the measurement from the falling edge of channel 1 to the rising edge of channel 3. This is shown in the lower portion of the following diagram:

Run the skew measurement by pressing the single button.



To determine the differential skew value, calculate the average of the absolute value of each of the mean of skew1 and the mean of skew2

Differential Skew = Avg (Abs(Mean(Skew 1), Abs(Mean(Skew2)))

Test TSG-04 - AC Common Mode Voltage

Purpose: To verify that the AC Common Mode Voltage of the PUT's transmitter is within the conformance limits.

References:

[1] SATA Standard, 7.2.1, Table 29 – Transmitted Signal Requirements
[2] Ibid, 7.2.2.3.5 – TX AC Common Mode Voltage (Gen2i, Gen1x, Gen2x)
[3] Ibid, 7.4.17 – TX AC Common Mode Voltage
[4] SATA unified test document, 2.12.4

Resource Requirements:

See appendix A.

Last Template Modification: April 12, 2006 (Version 1.0)

Discussion:

Reference [1] specifies the Transmitted Signal conformance limits for SATA PUTs. This specification includes conformance limits for the TX AC Common Mode Voltage. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

Test Setup:

Connect equipment as shown in Appendix B, figure 1A or 2A as appropriate. Note that it is only acceptable to use two single ended SMA connections for these measurements.

Test Procedure:

Using techniques and equipment as described in Appendix A of the PRE-TEST MOI, or equivalent, place the PUT in BISTFIS mode transmitting an MFTP pattern. Depending on the capability of the PUT, and the equipment available, it is acceptable to use either BIST-T or BIST-L to produce the needed test pattern.

If the PUT supports disconnects, remove the SATA PRE-TEST system, and connect SATA test fixture. Some PUTs require that the connection not be broken after BIST has been activated. In these situations, it may be necessary to use power splitters to allow simultaneous connection of the PRE-TEST system and the test equipment. Refer to Appendix A of the PRE-TEST MOI for additional details.

Start RT-Eye application on Scope. Select SATA module under "Modules" menu item. Select AC CM Voltage from the Amplitude measurements menu. Refer to the detailed procedure below.

Gen2: use MFTP 3.0 Gbps and select gen2 in the measurement configuration.

This is only done for Gen2 PUTs. Testing with SSC is optional.

Test pattern(s):	**SATA usage model:**
MFTP (SSC optional)	Gen2i/m

Gen2: 4 us/div, 25 ps/pt (> 100,000 UI)

Observable Results:

The AC Common Mode Voltage value shall be less than or equal to 50 mVp-p for Gen2i and Gen2m PUTs.

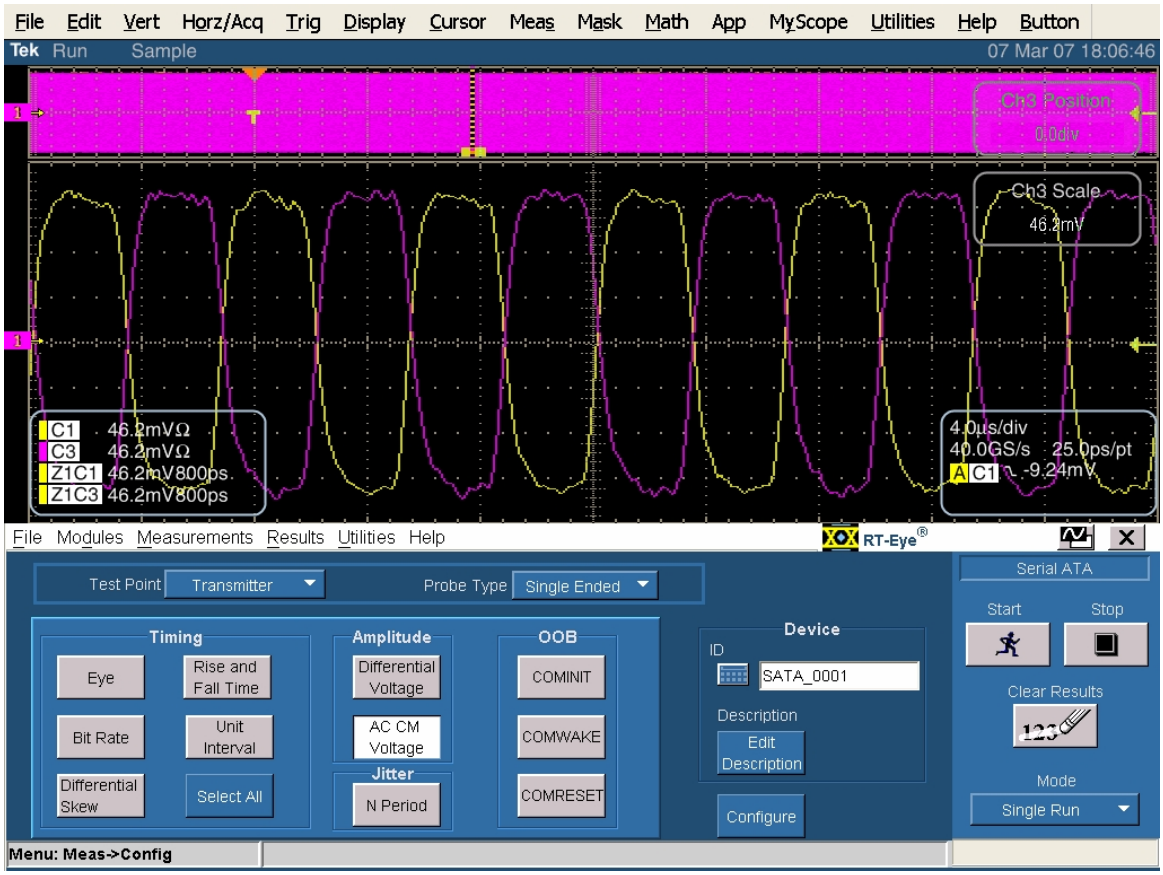
Accuracy: 0.25 % (Full Scale) rms

Possible Problems:

Detailed Procedure:

Start RT-Eye application on Scope. Select SATA module under “Modules” menu item. Select “AC CM Voltage” in Amplitude frame.

Select correct probe type.

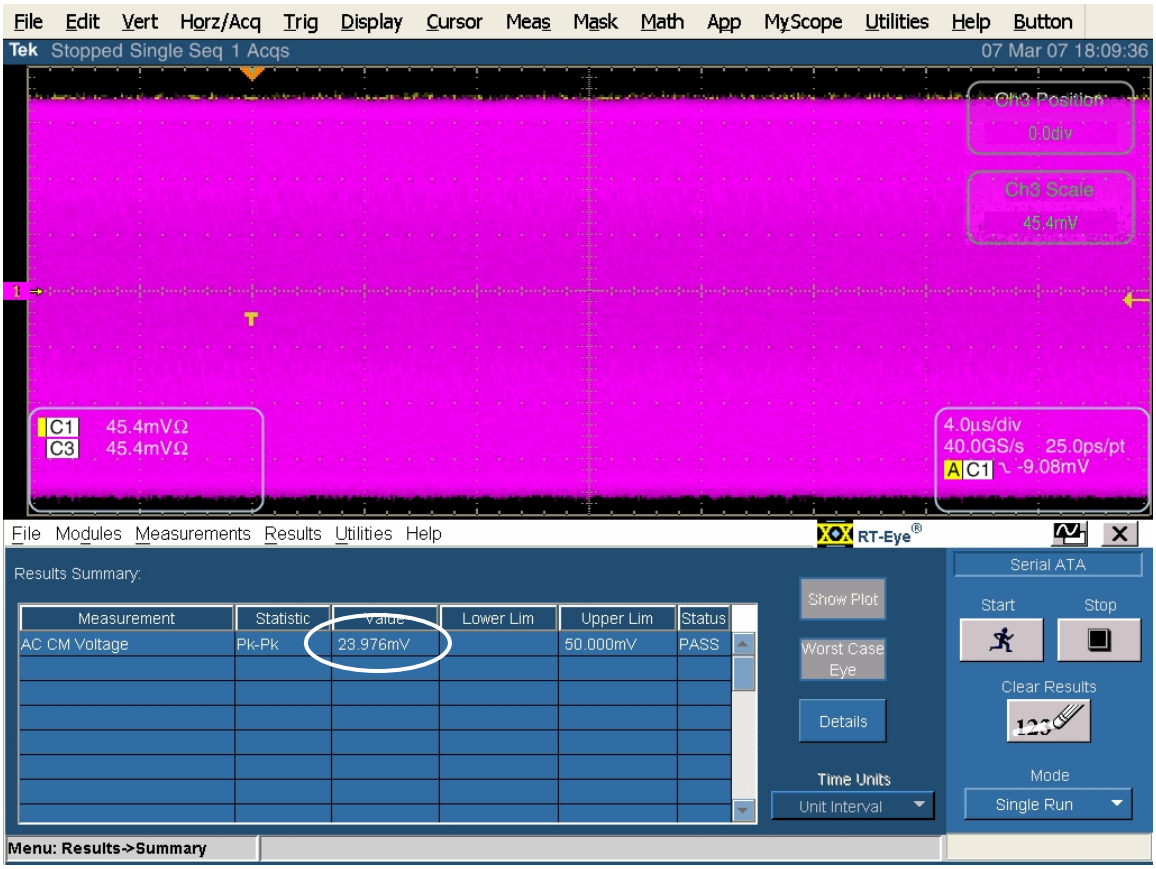


Click on Configure.

Select Source tab for source configuration. Select BIST FIS/User test method. Select correct source type and channels.

Select General Config tab for additional configuration. Set Usage Model to “Gen2i”. Set device type as appropriate.

Click on “Start” to run the test. Record the Pk-Pk Common Mode Voltage as shown below.



Verify that the AC Common Mode voltage is less than or equal to 50mV Pk-Pk.

Test TSG-05 - Rise/Fall Imbalance

Purpose: To verify that the Rise/Fall Imbalance of the PUT's transmitter is within the conformance limits.

References:

[1] SATA Standard, 7.2.1, Table 29 – Transmitted Signal Requirements
[2] Ibid, 7.2.2.3.9 – TX Rise/Fall Imbalance
[3] Ibid, 7.4.16 – TX Rise/Fall Imbalance
[4] SATA unified test document, 2.12.5

Resource Requirements:

See appendix A.

Last Template Modification: April 12, 2006 (Version 1.0)

Discussion:

Reference [1] specifies the Transmitted Signal conformance limits for SATA PUTs. This specification includes conformance limits for the Rise/Fall Imbalance. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

Test Setup:

Connect equipment as shown in Appendix B, figure 1A or 2A as appropriate. Single ended measurements using SMA cables are recommended.

Test Procedure:

Using techniques and equipment as described in Appendix A of the PRE-TEST MOI, or equivalent, place the PUT in BISTFIS mode transmitting an HFTP pattern. Depending on the capability of the PUT, and the equipment available, it is acceptable to use either BIST-T or BIST-L to produce the needed test pattern.

If the PUT supports disconnects, remove the SATA PRE-TEST system, and connect SATA test fixture. Some PUTs require that the connection not be broken after BIST has been activated. In these situations, it may be necessary to use power splitters to allow simultaneous connection of the PRE-TEST system and the test equipment. Refer to Appendix A of the PRE-TEST MOI for additional details.

Start JIT3 application on Scope. Cancel the Jitter Wizard and within JIT3 go to File, Recall 'SATA gen2 rise fall imbalance setup' or use the combined setup 'SATA skew_RF imb_amp imb ref wfm'. Select rise and fall time for both channels from the General measurements menu. See the following detailed procedure for additional information.

This is only done for Gen2 devices. Testing with SSC is optional.

Repeat the PRE-TEST procedure and measurement for MFTP.

Test pattern(s):	**SATA usage model:**
HFTP, MFTP (SSC optional)	Gen2i/m

Gen2: 4 us/div, 25 ps/pt (> 100,000 UI)

Observable Results:

The Rise/Fall Imbalance value shall be less than 20% for Gen2i and Gen2m PUTs.

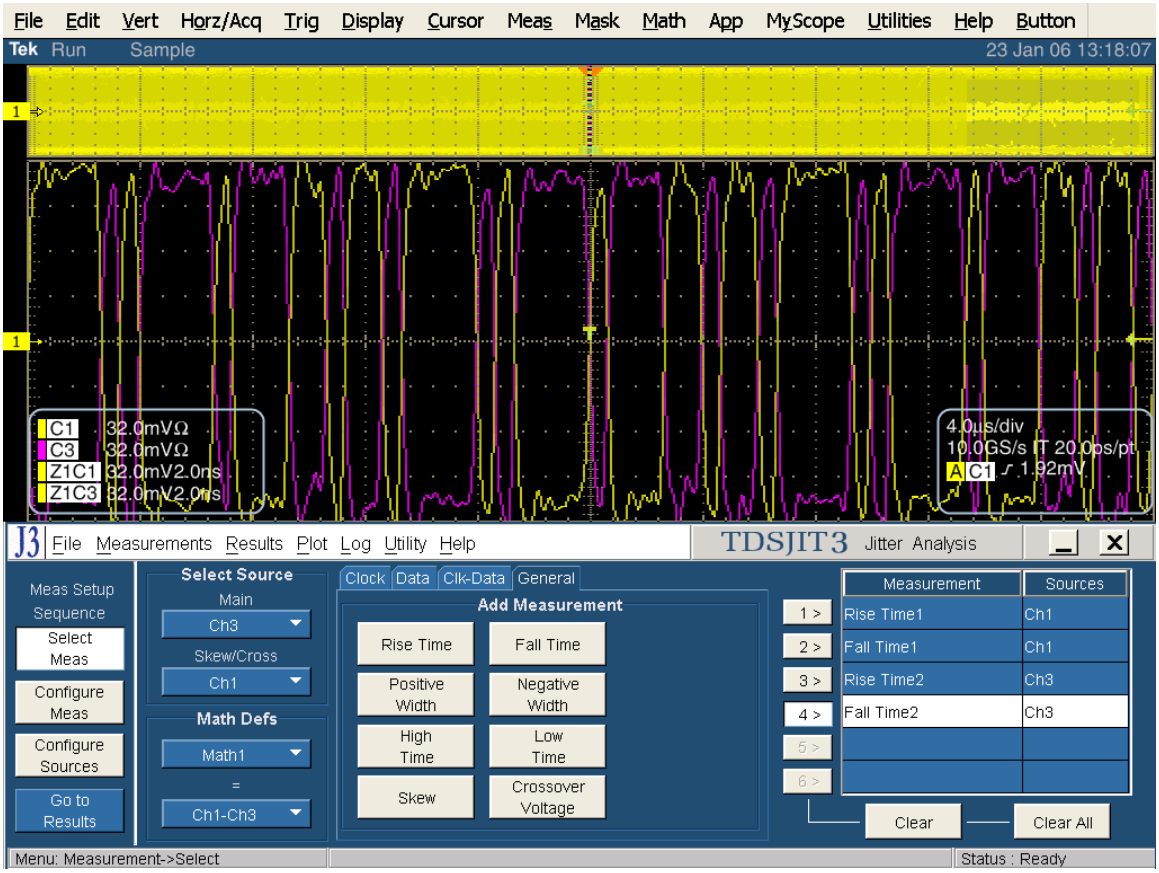
Accuracy: < 1.6 % typical gen2

Possible Problems:

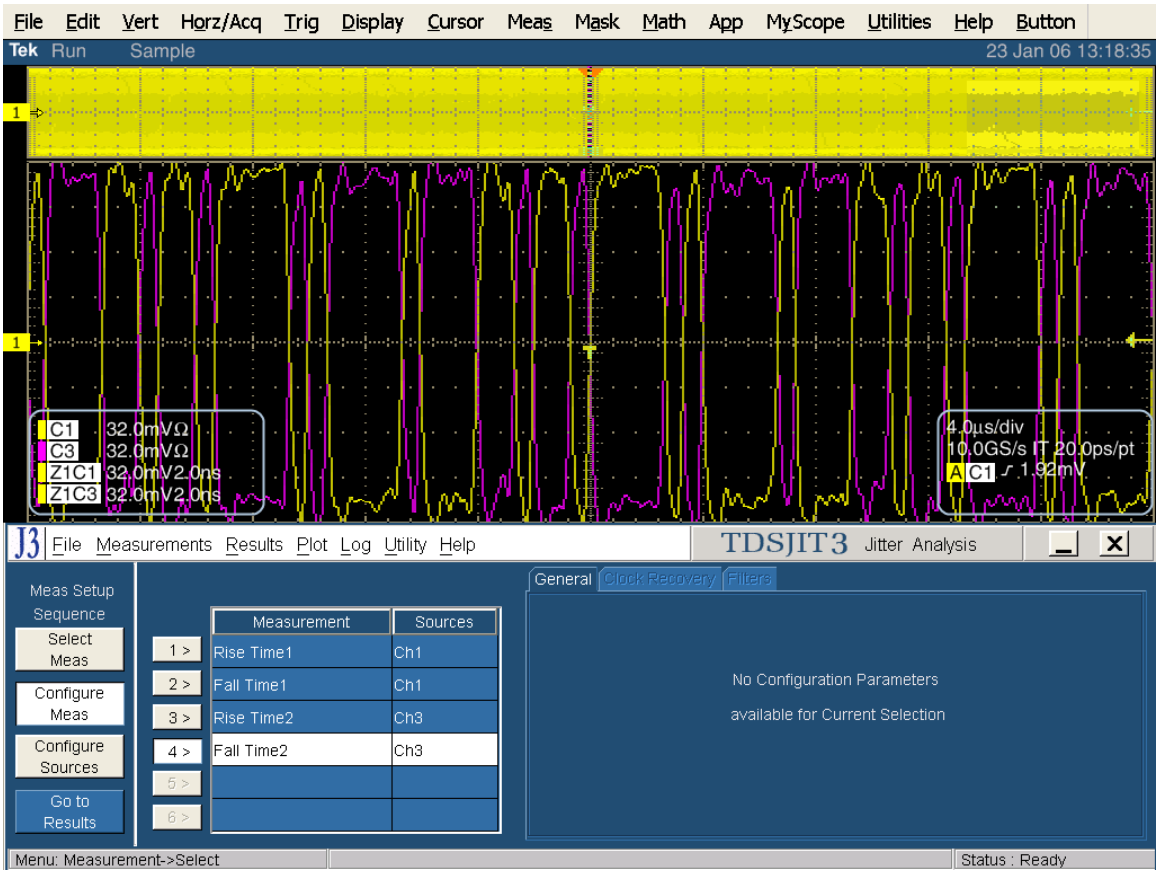
Detailed Procedure:

Run JIT3 version 2 by selecting App, Jitter Analysis – Advanced, from the Oscilloscope menu.

Select rise and fall time for both channel 1 and 3 under the General tab.



The measurement configuration is default.

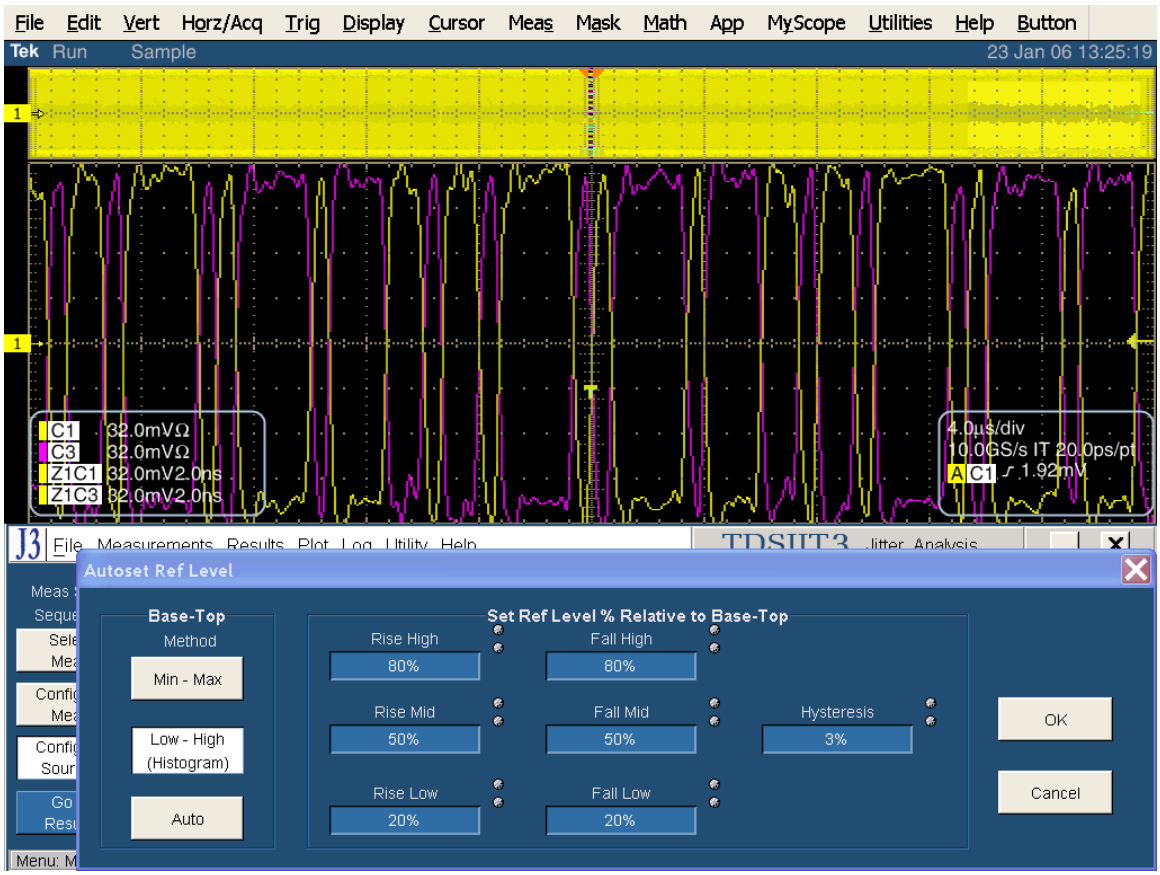


Under configure sources, select the Ref levels tab.

Select Ch1 and press the Setup button.

Select 20 and 80 % for both rise and fall time, and select Low – High (Histogram).

Press OK.

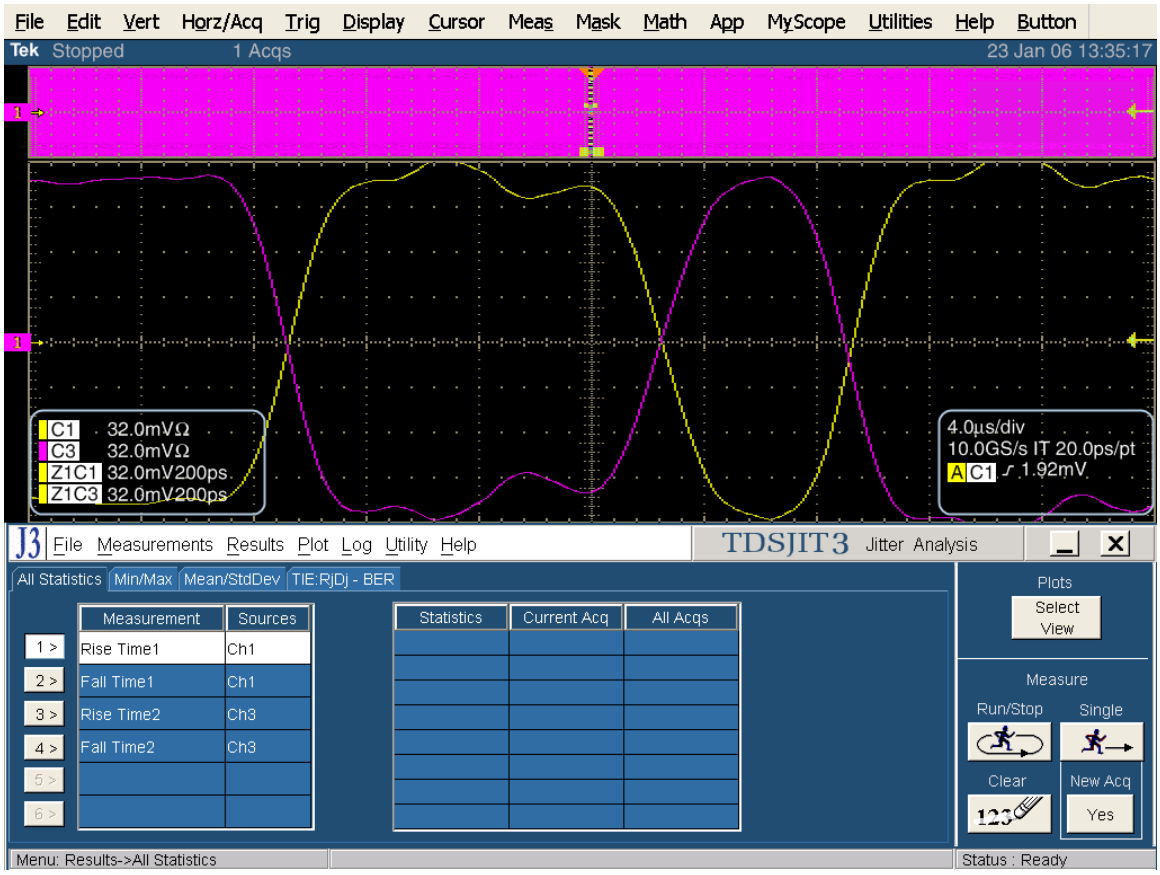


Now select Ch3 (under Configure Sources Ref levels) and press the Setup button.

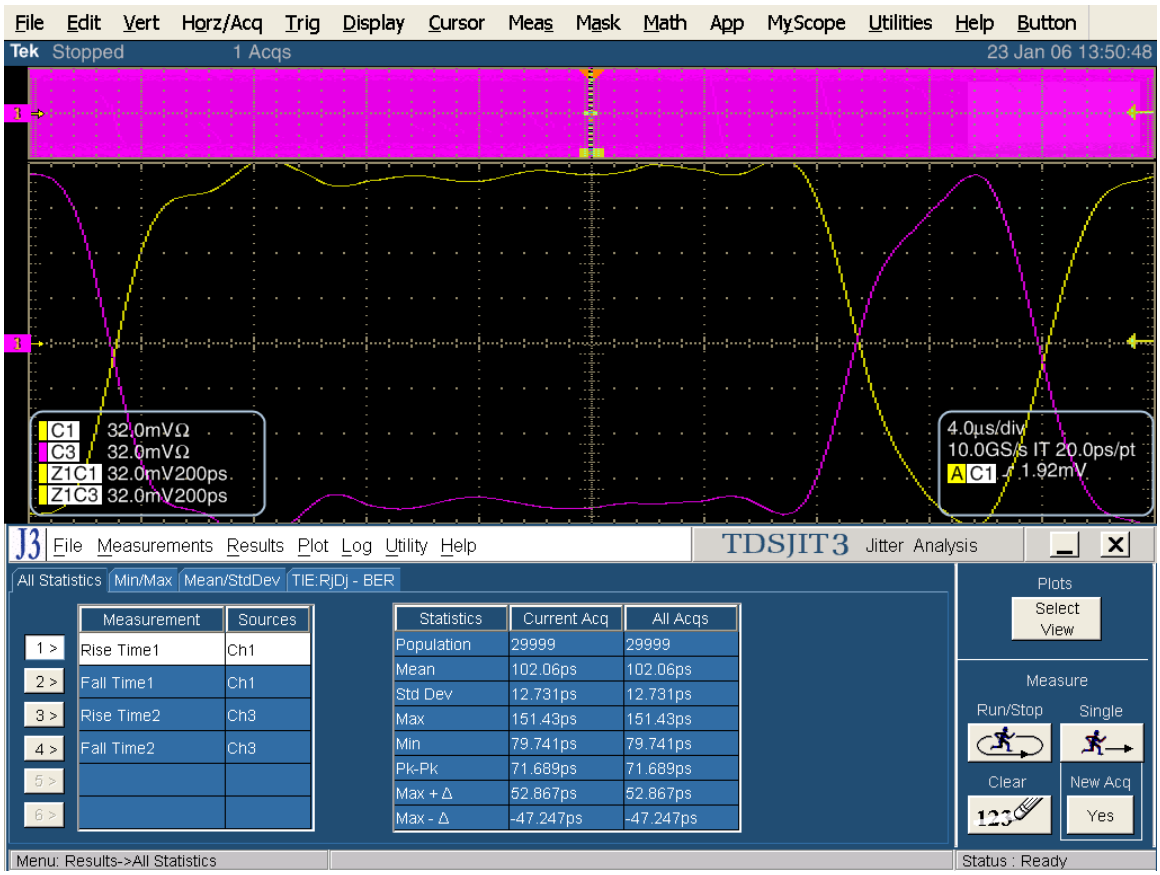
Select 20 and 80 % for both rise and fall time, and select Low – High (Histogram).

Press OK.

Click on Go to Results and press the Single button.



From All Statistics take the mean values from rise time 1, fall time 1, rise time 2, fall time 2. Use these values to calculate the rise fall imbalance parameter. See below.



Imbalance TX+r to TX-f: [%] = 100*ABS(2*(rise time1-fall time2)/(rise time1+fall time2));
Imbalance TX+f to TX-r: [%] = 100*ABS(2*(fall time1-rise time2)/(fall time1+rise time2));

Note: the imbalance has to be divided by the average of rise and fall time, hence the factor 2 in the equation.

Test TSG-06 - Amplitude Imbalance

Purpose: To verify that the Amplitude Imbalance of the PUT's transmitter is within the conformance limits.

References:

[1] SATA Standard, 7.2.1, Table 29 – Transmitted Signal Requirements
[2] Ibid, 7.2.2.3.10 – TX Amplitude Imbalance (Gen2i, Gen1x, Gen2x)
[3] Ibid, 7.4.15 – TX Amplitude Imbalance
[4] SATA unified test document, 2.12.6

Resource Requirements:

See appendix A.

Last Template Modification: April 12, 2006 (Version 1.0)

Discussion:

Reference [1] specifies the Transmitted Signal conformance limits for SATA PUTs. This specification includes conformance limits for the TX Amplitude Imbalance. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

Test Setup:

Connect equipment as shown in Appendix B, figure 1A or 2A as appropriate. Single ended measurements using SMA cables are recommended.

Test Procedure:

Using techniques and equipment as described in Appendix A of the PRE-TEST MOI, or equivalent, place the PUT in BISTFIS mode transmitting an HFTP pattern. Depending on the capability of the PUT, and the equipment available, it is acceptable to use either BIST-T or BIST-L to produce the needed test pattern.

If the PUT supports disconnects, remove the SATA PRE-TEST system, and connect SATA test fixture. Some PUTs require that the connection not be broken after BIST has been activated. In these situations, it may be necessary to use power splitters to allow simultaneous connection of the PRE-TEST system and the test equipment. Refer to Appendix A of the PRE-TEST MOI for additional details.

Perform measurement using integrated measurement capability of scope. Recall instrument setup 'SATA gen2 Amp_Imbal'. See the following detailed procedure for additional information.

This test is only performed on Gen2 PUTs.

Repeat the PRE-TEST procedure and test for MFTP. Note that for MFTP, only the 2nd bit (non-transition) should be included in the analysis.

Test pattern(s):	**SATA usage model:**
HFTP, MFTP (SSC optional)	3Gbps (Gen2i and Gen2m)

Gen2: 4 us/div, 25 ps/pt (> 100,000 UI)

Observable Results:

The TX Amplitude Imbalance value shall be less than 10%.

Accuracy: < 0.5 % rms

Possible Problems:

Detailed Procedure:
Set scope to 100ps/div, 40GS/s, 500fs/pt
Set scope trigger to CH1, Edge. Adjust trigger level for 0V.
Set Horizontal Position to 50%
Select Meas from the Oscilloscope menu, and click on "Measurement Setup…".
Click on the Histogram tab.
Select Wfm Ct.

Click on "Ref Levs" under "Setup" column
Make sure that the High Ref = 80 % and Low Ref = 20 % for both measurements.
Click on the "Setup" button in the lower right corner to return to the Setup screen.

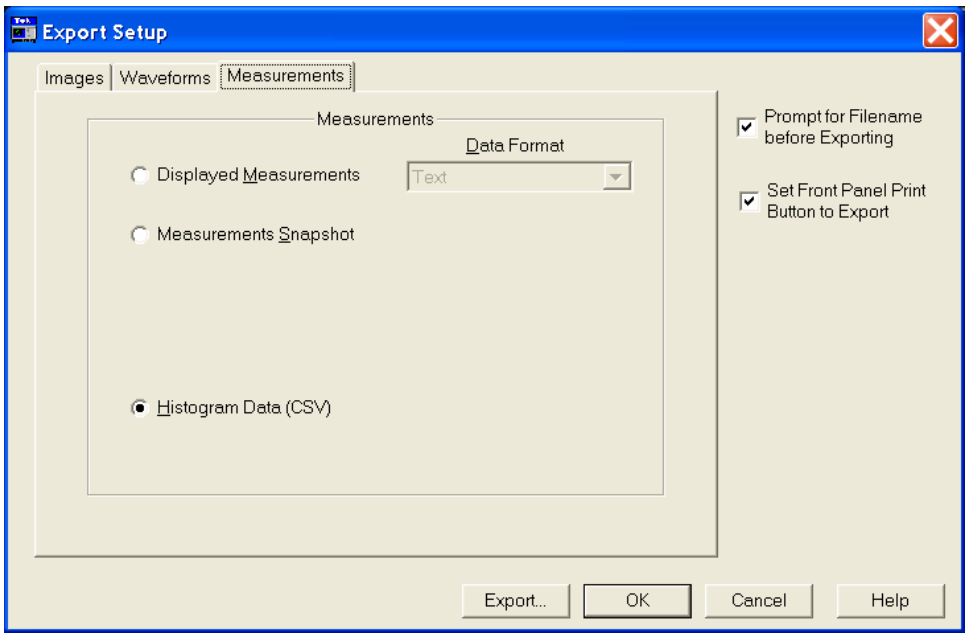
Click on "Histogram" button under "Display" column
Select CH1 for source.
Select "Vert" for Histogram Mode
Use the limits settings to set the histogram location and size on the waveform. The measurement is to be made from .45UI to .55UI. The following table describes the values to use for HFTP measurements:

	D+ High	D+ Low	D- High	D- Low
Left Limit	150ps	-183ps	-183ps	150ps
Right Limit	183ps	-150ps	-150ps	183ps
Top Limit	197mV	0V	197mV	0V
Bottom Limit	0V	-197mV	0V	-197mV

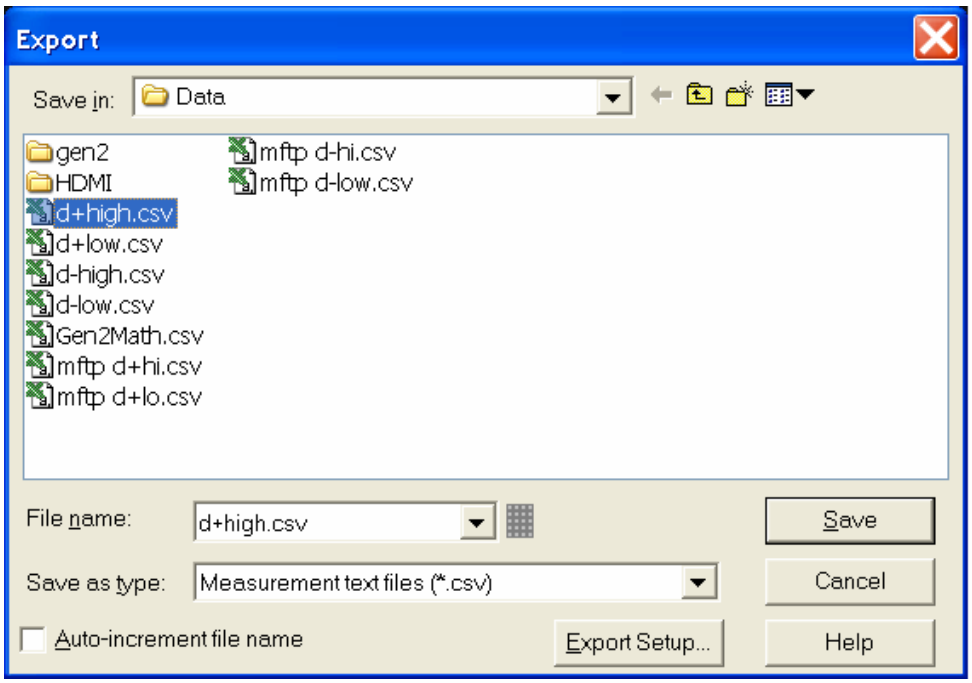
The following view shows a typical HFTP waveform, and the histogram set for D+ High acquisition:

Allow this to run until the waveform counter shows 10,000 waveforms acquired. Press “Run/Stop” button on the front panel to stop the acquisition at 10,000.

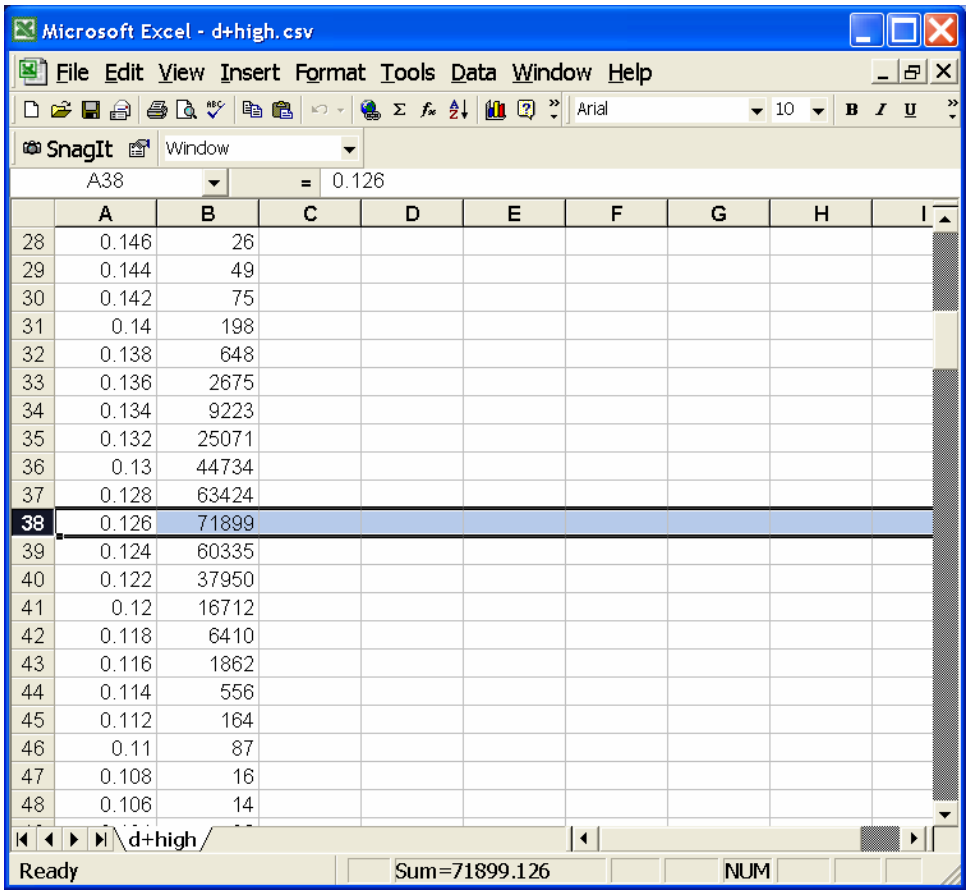
To determine the mode (most prevalent value), export the histogram data. This can be done by clicking on the “File” menu item, then selecting “Export Setup”. Choose the “Measurements” tab, and click on the “Histogram Data” radio button.



Click on the "Export…" button to save the data, and save the file using some recognizable name.



Once this is complete, the histogram data file can be opened, and the mode determined by the highest count for a particular value. The following is an example:



	A	B
28	0.146	26
29	0.144	49
30	0.142	75
31	0.14	198
32	0.138	648
33	0.136	2675
34	0.134	9223
35	0.132	25071
36	0.13	44734
37	0.128	63424
38	0.126	71899
39	0.124	60335
40	0.122	37950
41	0.12	16712
42	0.118	6410
43	0.116	1862
44	0.114	556
45	0.112	164
46	0.11	87
47	0.108	16
48	0.106	14

Repeat this procedure for the other 3 values. Record the voltage values for each of the 4 mode values.

Once all four measurements have been made, calculate the amplitude for each channel:

Ch1 amp = Mode reading (D+ Hi) – Mode reading (D+Low)
Ch3 amp = Mode reading (D- Hi) – Mode reading (D-Low)

From this, the imbalance can be calculated:

Imbalance [%] = 100*ABS[2*(Ch1 amp – CH3 amp)/(CH1 amp + CH3 amp)]

Repeat the procedure described above for HFTP to make the MFTP measurement.

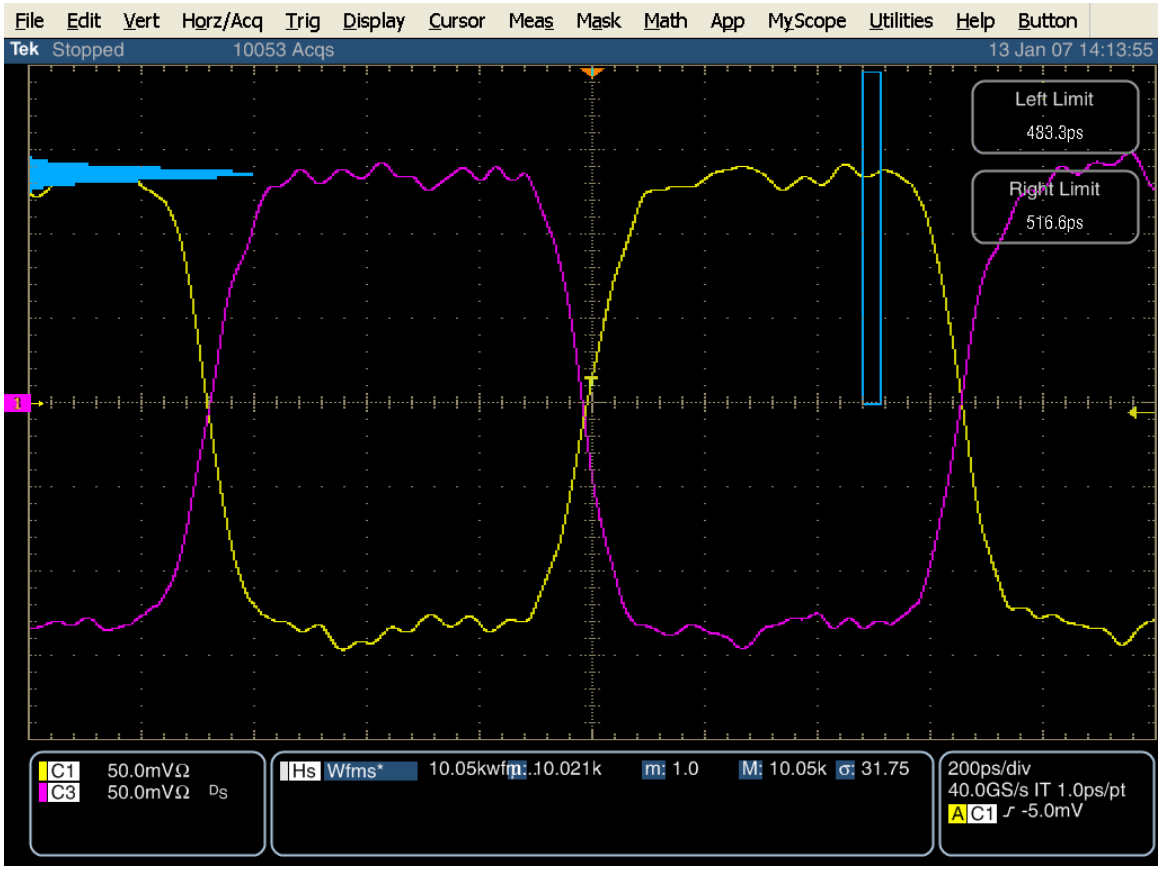
Set the PUT to transmit an MFTP signal.

Change the scope setting to 200ps/div, 40GS/s, and 500fs/pt

The MFTP test requires only testing the non-transition bit (bit 2). Therefore, it is necessary to alter the histogram limit values to get the histogram properly located on the waveform. The following table describes the values to use for MFTP measurements:

	D+ High	D+ Low	D- High	D- Low
Left Limit	483ps	-183ps	-183ps	483ps
Right Limit	516ps	-150ps	-150ps	516ps
Top Limit	197mV	0V	197mV	0V
Bottom Limit	0V	-197mV	0V	-197mV

The following diagram shows making the D+ High measurement:



The following diagram shows making the D- High measurement:

As with the HFTP test, acquire 10,000 waveforms at each of the four histogram locations. Record each of the four mode values.

Once all four measurements have been made, calculate the amplitude for each channel:

Ch1 amp = Mode reading (D+ Hi) – Mode reading (D+Low)
Ch3 amp = Mode reading (D- Hi) – Mode reading (D-Low)

From this, the imbalance can be calculated:

Imbalance [%] = 100*ABS[2*(Ch1 amp – CH3 amp)/(CH1 amp + CH3 amp)]

Test TSG-07 - TJ at Connector, Clock to Data, $f_{BAUD}/10$ (Obsolete)

Purpose: To verify that the TJ at Connector (Clock to Data, $f_{BAUD}/10$) of the PUT's transmitter is within the conformance limits.

NOTE: This test is no longer required by the SATA Unified Test Document, and per ECN #006. It is provided here as a historical reference.

References:

[1] SATA Standard, 7.2.1, Table 22 – Transmitted Signal Requirements
[2] Ibid, 7.2.2.3.11
[3] Ibid, 7.4.8
[4] SATA unified test document, 2.12.7

Resource Requirements:

See appendix A.

Last Template Modification: May 15, 2006 (Version 1.0)

Discussion:

Reference [1] specifies the Transmitted Signal conformance limits for SATA devices. This specification includes conformance limits for the TJ at Connector (Clock to Data, $f_{BAUD}/10$). Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

Test Setup:

Connect equipment as shown in Appendix B, figure 1 or 2 as appropriate. Note that it is acceptable to use either differential or pseudo-differential (single ended plus math waveform) probes for these measurements.

Test Procedure:

Using techniques and equipment as described in Appendix A of the PRE-TEST MOI, or equivalent, place the PUT in BISTFIS mode transmitting an HFTP pattern. Depending on the capability of the PUT, and the equipment available, it is acceptable to use either BIST-T or BIST-L to produce the needed test pattern.

If the PUT supports disconnects, remove the SATA PRE-TEST system, and connect SATA test fixture. Some PUTs require that the connection not be broken after BIST has been activated. In these situations, it may be necessary to use power splitters to allow simultaneous connection of the PRE-TEST system and the test equipment. Refer to Appendix A of the PRE-TEST MOI for additional details.

Start JIT3 application on Scope. Recall the setup: 'SATA jitter gen1' or 'SATA jitter gen1 ref wfm'. See the following detailed procedure for additional information. Note: the setup files will configure JIT3 to perform all measurements for TSG-07, TSG-08, TSG-09, and TSG-10 for the test pattern being used. Therefore, it is only necessary to run the JIT3 analysis 2 times (once for HFTP, and once for LBP) to acquire all data needed for TSG-07 through TSG-10.

This test is only performed on Gen1 devices. Repeat PRE-TEST procedure and test using LBP. SSOP is optional. SSC is optional for this test.

Test pattern(s):	**SATA usage model:**
HFTP , LBP , (SSOP is optional) (SSC optional)	1.5Gbps (Gen1) PUTs that support 3Gbps should be tested at 1.5Gbps for this test

Gen1: 10 us/div, 25 ps/pt (> 100,000 UI)

Observable Results:

NOTE: This test is informative only at this time, and will not affect pass/fail status of PUT.

The TJ at Connector (Clock to Data, $f_{BAUD}/10$) value shall be less than 0.30 UI for 1.5Gbps PUTs.

Accuracy: estimated JNF is 2 ps rms

Possible Problems:

Per ECN-18, a new LBP pattern was defined that eliminates the disparity ambiguity, as described below. Use ECN-18 compliant LBP for performing the amplitude test whenever possible.

If an ECN-18 LBP is not available, it is possible to use the older LBP pattern. However, a pattern mismatch error can occur. To avoid the pattern mismatch problem, make sure that the real lone bit pattern with positive disparity is used (0011 0110 1111 0100 0010 0011 0110 1111 0100 0010 0011 0110 etc….).
This pattern has a lone '1' bit between 4 '0's and 3 '0's, and is required for the algorithm. Visually verify the proper disparity on LBP by zooming in on the acquired waveform, and inspecting the waveform for a section that contains a "0001000" section. If this pattern is not readily apparent, re-load the LBP BISTFIS pattern into the PUT, and reacquire the waveform, then repeat the inspection until the proper pattern is seen. Once the proper pattern is detected, continue running the test. It is only necessary to make this inspection on LBP patterns, as there is a 50% chance of getting the desired positive disparity each time the LBP is loaded into the PUT.

Detailed Procedure:

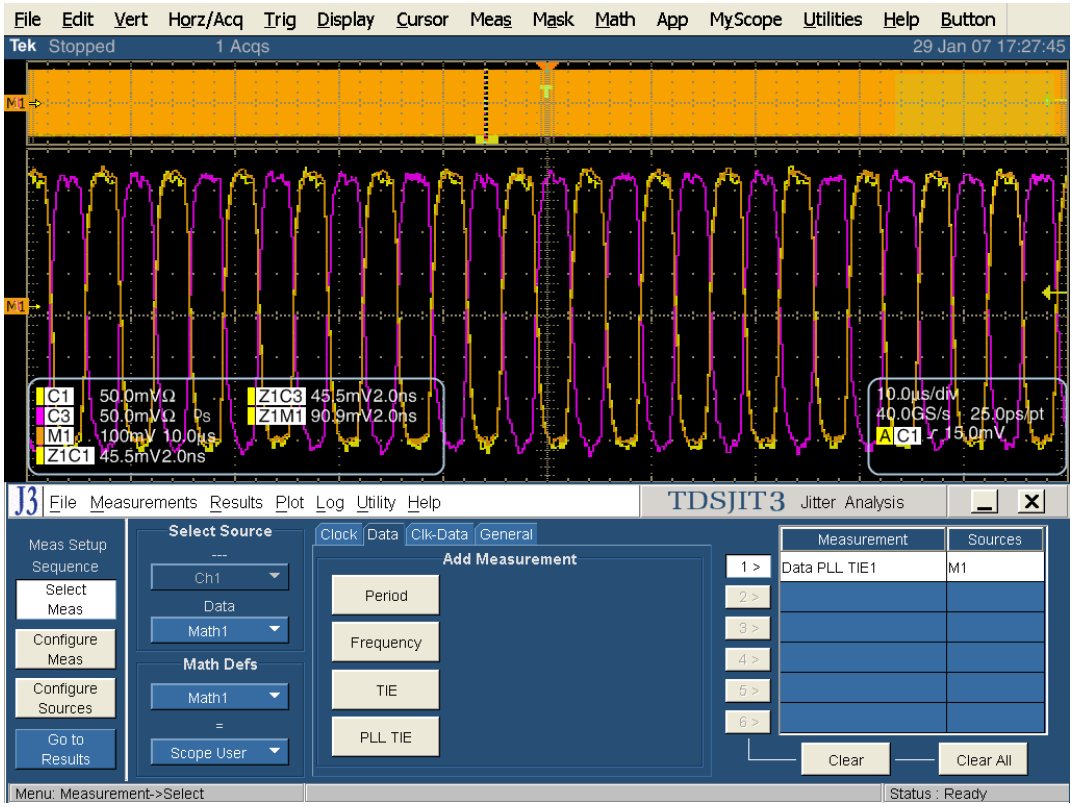
Scope setup: 10 us/div, 25 ps/pt (Recall Instrument Setup from file ‘SATA gen1 setup standard.set’)

Run JIT3 version 2 by selecting App, Jitter Analysis – Advanced, from the Oscilloscope menu.

Cancel Jitter Wizard.

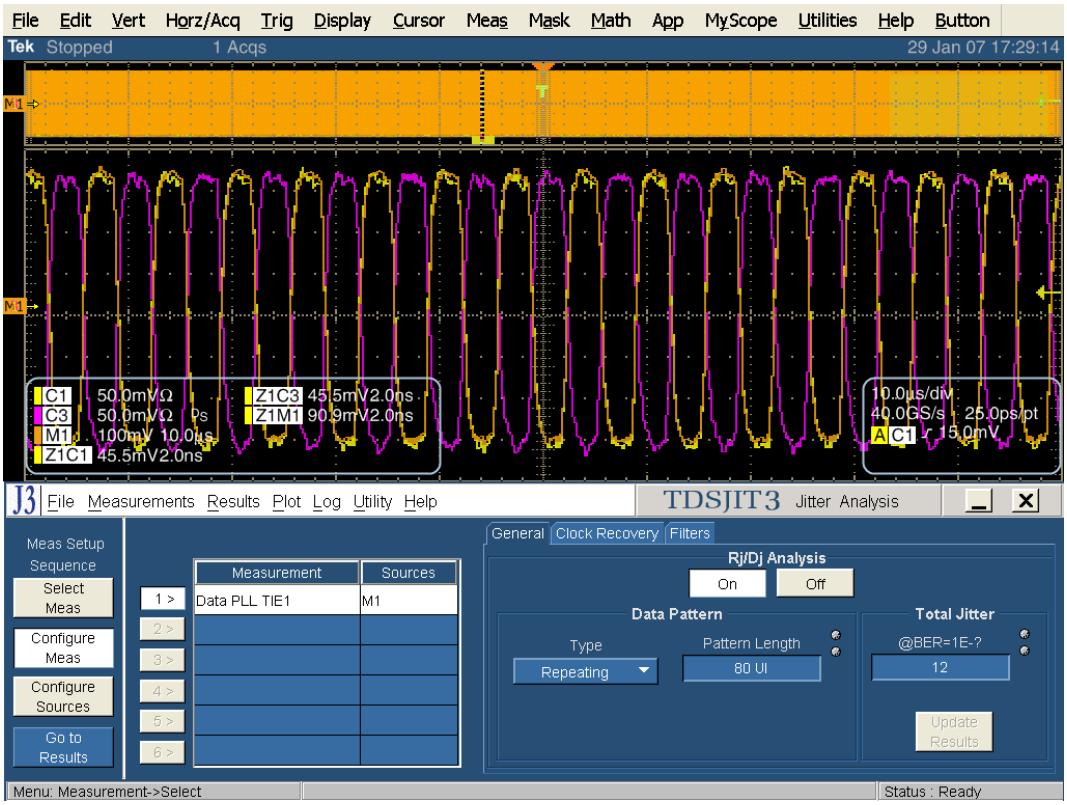
Define Data channel as Math1 = Ch1 – Ch3.

Select Data PLL-TIE1 (Source M1) from measurement menu.

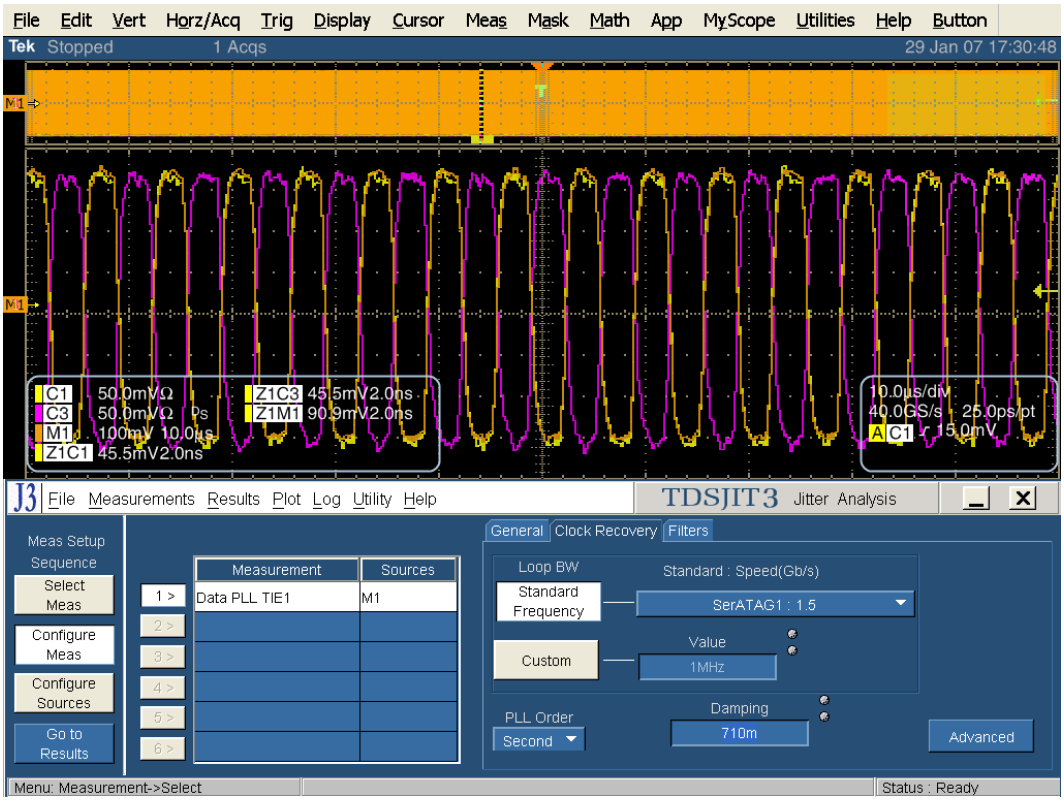


Configure Data PLL-TIE 1 by selecting “Configure Meas”:

General: select Repeating Data Pattern, and window length set to 80 UI.



Clock recovery: Loop BW standard frequency SerATAG1 : 1.5, PLL Order : Second, and Damping to .710.



Clock recovery advanced: click on advanced

Set nominal data rate: 1.5 Gbps

Filters: 2nd order high pass, 150 MHz

Then Go to results and press the Single button.

The Tj result will be under the TIE:RjDj – BER tab.

Test TSG-08 - DJ at Connector, Clock to Data, $f_{BAUD}/10$ (Obsolete)

Purpose: To verify that the DJ at Connector (Clock to Data, $f_{BAUD}/10$) of the PUT's transmitter is within the conformance limits.

NOTE: This test is no longer required by the SATA Unified Test Document, and per ECN #006. It is provided here as a historical reference.

References:

[1] SATA Standard, 7.2.1, Table 22 – Transmitted Signal Requirements
[2] Ibid, 7.2.2.3.11
[3] Ibid, 7.4.8
[4] SATA unified test document, 2.12.8

Resource Requirements:

See appendix A.

Last Template Modification: May 15, 2006 (Version 1.0)

Discussion:

Reference [1] specifies the Transmitted Signal conformance limits for SATA devices. This specification includes conformance limits for the DJ at Connector (Clock to Data, $f_{BAUD}/10$). Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

Test Setup:

Connect equipment as shown in Appendix B, figure 1 or 2 as appropriate. Note that it is acceptable to use either differential or pseudo-differential (single ended plus math waveform) probes for these measurements.

Test Procedure:

Using techniques and equipment as described in Appendix A of the PRE-TEST MOI, or equivalent, place the PUT in BISTFIS mode transmitting an HFTP pattern. Depending on the capability of the PUT, and the equipment available, it is acceptable to use either BIST-T or BIST-L to produce the needed test pattern.

If the PUT supports disconnects, remove the SATA PRE-TEST system, and connect SATA test fixture. Some PUTs require that the connection not be broken after BIST has been activated. In these situations, it may be necessary to use power splitters to allow simultaneous connection of the PRE-TEST system and the test equipment. Refer to Appendix A of the PRE-TEST MOI for additional details.

Start JIT3 application on Scope. Recall the setup: 'SATA jitter gen1' or 'SATA jitter gen1 ref wfm'. **See Detailed Procedure in TSG-07 for additional information pertaining to TSG-08.** Note: the setup files will configure JIT3 to perform all measurements for TSG-07, TSG-08, TSG-09, and TSG-10 for the test pattern being used. Therefore, it is only necessary to run the JIT3 analysis 2 times (once for HFTP, and once for LBP) to acquire all data needed for TSG-07 through TSG-10.

This test is only performed on Gen1 devices. Repeat PRE-TEST procedure and test using LBP. SSOP is optional. SSC is optional for this test.

Test pattern(s):	**SATA usage model:**
HFTP and LBP. SSOP is optional. (SSC optional)	1.5Gbps (Gen1) PUTs that support 3Gbps should be tested at 1.5Gbps for this test

Gen1: 10 us/div, 25 ps/pt (> 100,000 UI)

Observable Results:

NOTE: This test is informative only at this time, and will not affect pass/fail status of PUT.

The DJ at Connector (Clock to Data, $f_{BAUD}/10$) value shall be less than 0.17 UI for 1.5Gbps PUTs.

Accuracy: estimated JNF is 2 ps rms

Possible Problems:
See LBP discussion in TSG-07 "Possible Problems" section.

Detailed Procedure:

Utilize the procedure described in TSG-07. The results for TSG-08 are available on the same display used to capture TSG-07 results. The following screen capture shows the location of the reading:

Test TSG-09 - TJ at Connector, Clock to Data, $f_{BAUD}/500$

Purpose: To verify that the TJ at Connector (Clock to Data, $f_{BAUD}/500$) of the PUT's transmitter is within the conformance limits.

References:

[1] SATA Standard, 7.2.1, Table 29 – Transmitted Signal Requirements
[2] Ibid, 7.2.2.3.11
[3] Ibid, 7.4.8
[4] SATA unified test document, 2.12.9

Resource Requirements:

See appendix A.

Last Template Modification: May 15, 2006 (Version 1.0)

Discussion:

Reference [1] specifies the Transmitted Signal conformance limits for SATA PUTs. This specification includes conformance limits for the TJ at Connector (Clock to Data, $f_{BAUD}/500$). Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

Note: Prior to making this jitter measurement, it is necessary to follow the procedure in Appendix G, and determine the proper settings to use for Gen1 loop bandwidth in JIT3. The resulting loop bandwidth setting must be used for all Gen1 jitter measurements.

Test Setup:

Connect equipment as shown in Appendix B, figure 1 or 2 as appropriate. Note that it is acceptable to use either differential or pseudo-differential (single ended plus math waveform) probes for these measurements.

Test Procedure:

Using techniques and equipment as described in Appendix A of the PRE-TEST MOI, or equivalent, place the PUT in BISTFIS mode transmitting an HFTP pattern. Depending on the capability of the PUT, and the equipment available, it is acceptable to use either BIST-T or BIST-L to produce the needed test pattern.

If the PUT supports disconnects, remove the SATA PRE-TEST system, and connect SATA test fixture. Some PUTs require that the connection not be broken after BIST has been activated. In these situations, it may be necessary to use power splitters to allow simultaneous connection of the PRE-TEST system and the test equipment. Refer to Appendix A of the PRE-TEST MOI for additional details.

Start JIT3 application on Scope. Recall the setup: 'SATA jitter gen1' or 'SATA jitter gen1 ref wfm'. Note: the setup files will configure JIT3 to perform all measurements for TSG-07, TSG-08, TSG-09, and TSG-10 for the test pattern being used. Therefore, it is only necessary to run the JIT3 analysis 2 times (once for HFTP, and once for LBP) to acquire all data needed for TSG-07 through TSG-10.

This test is only performed on Gen1 PUTs. Repeat PRE-TEST procedure and test using LBP. SSOP is optional. SSC is optional for this test.

Test pattern(s):	**SATA usage model:**
HFTP and LBP. SSOP is optional. (SSC optional)	1.5Gbps (Gen1i and Gen1m) PUTs that support 3Gbps should be tested at 1.5Gbps for this test

Gen1: 10 us/div, 25 ps/pt (> 100,000 UI)

Observable Results:

NOTE: This test is informative only at this time, and will not affect pass/fail status of PUT.

The TJ at Connector (Clock to Data, $f_{BAUD}/500$) value shall be less than 0.37 UI for 1.5Gbps PUTs.

Accuracy: estimated JNF is 2 ps rms

Possible Problems:

See LBP discussion in TSG-07 "Possible Problems" section.

Detailed Procedure:

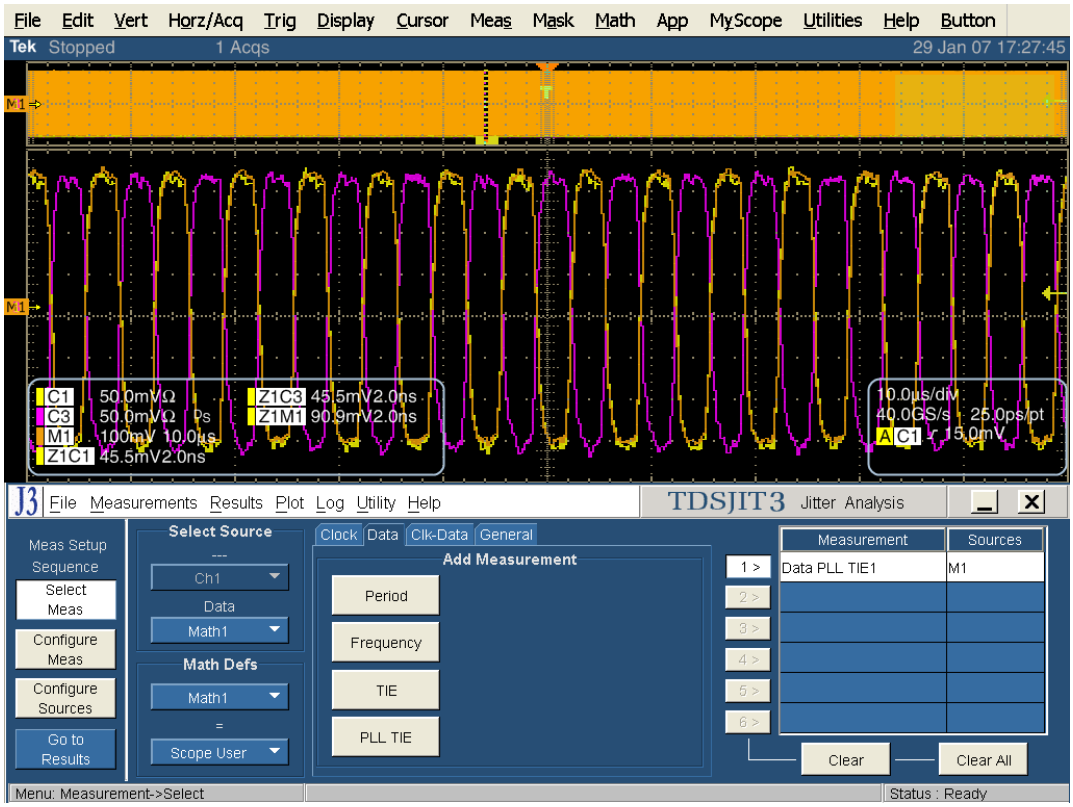
Scope setup: 10 us/div, 25 ps/pt (Recall Instrument Setup from file 'SATA gen1 setup standard.set')

Run JIT3 version 2 by selecting App, Jitter Analysis – Advanced, from the Oscilloscope menu.

Cancel Jitter Wizard.

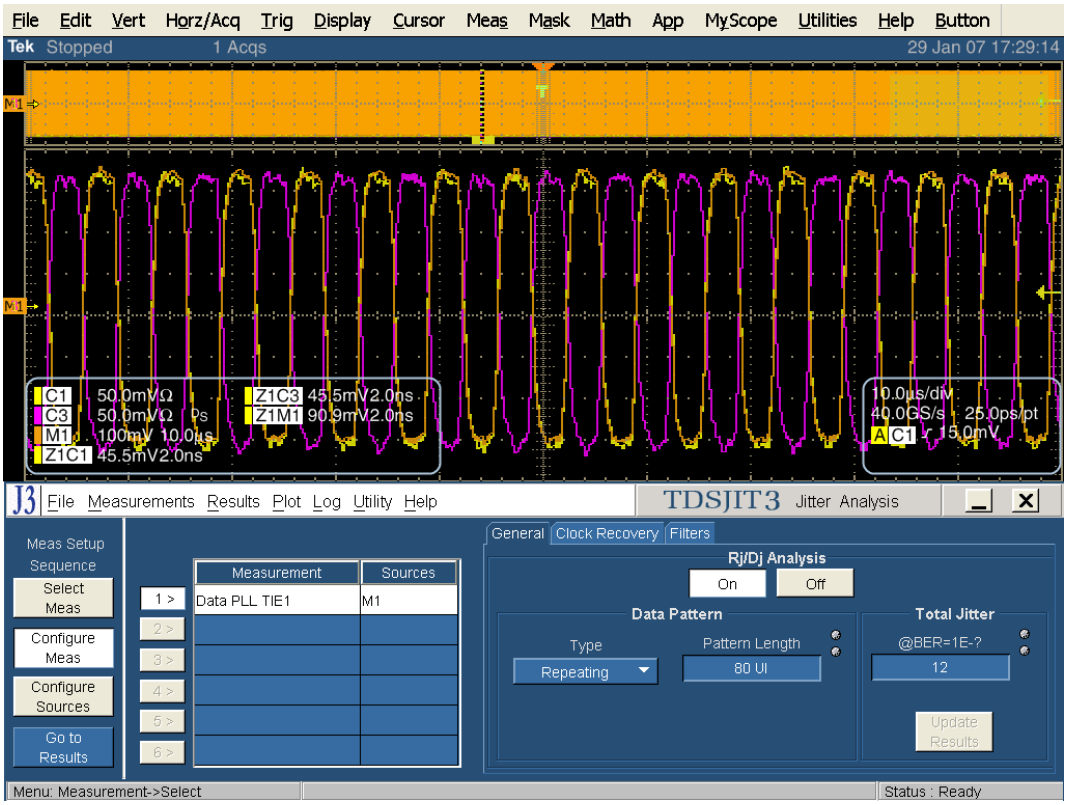
Define Data channel as Math1 = Ch1 – Ch3.

Select Data PLL-TIE1 (Source M1) from measurement menu.

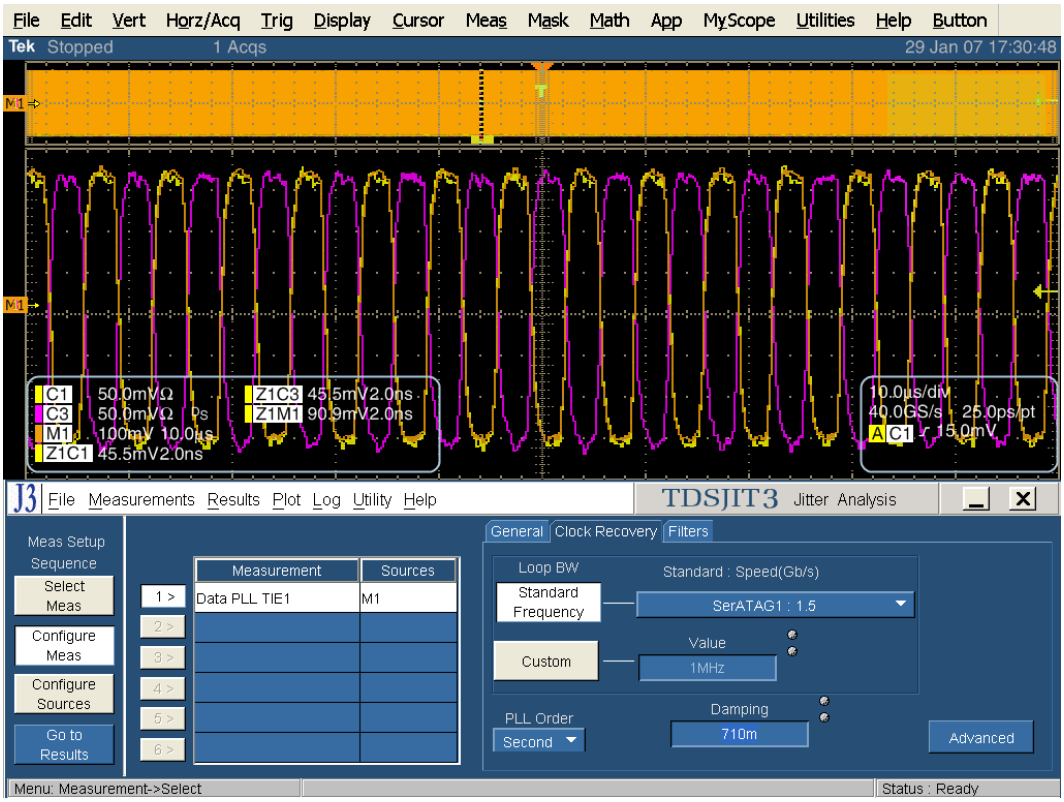


Configure Data PLL-TIE 1 by selecting “Configure Meas”:

General: select Repeating Data Pattern, and window length set to 80 UI.



Clock recovery: Loop BW custom (using value determined in Appendix G procedure), PLL Order : Second, and Damping to .710.



Clock recovery advanced: click on advanced

Set nominal data rate: 1.5 Gbps

Then Go to results and press the Single button.

The Tj result will be under the TIE:RjDj – BER tab.

Test TSG-10 - DJ at Connector, Clock to Data, $f_{BAUD}/500$

Purpose: To verify that the DJ at Connector (Clock to Data, $f_{BAUD}/500$) of the PUT's transmitter is within the conformance limits.

References:

[1] SATA Standard, 7.2.1, Table 29 – Transmitted Signal Requirements
[2] Ibid, 7.2.2.3.11
[3] Ibid, 7.4.8
[4] SATA unified test document, 2.12.10

Resource Requirements:

See appendix A.

Last Template Modification: May 15, 2006 (Version 1.0)

Discussion:

Reference [1] specifies the Transmitted Signal conformance limits for SATA PUTs. This specification includes conformance limits for the DJ at Connector (Clock to Data, $f_{BAUD}/500$). Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

Note: Prior to making this jitter measurement, it is necessary to follow the procedure in Appendix G, and determine the proper settings to use for Gen1 loop bandwidth in JIT3. The resulting loop bandwidth setting must be used for all Gen1 jitter measurements.

Test Setup:

Connect equipment as shown in Appendix B, figure 1 or 2 as appropriate. Note that it is acceptable to use either differential or pseudo-differential (single ended plus math waveform) probes for these measurements.

Test Procedure:

Using techniques and equipment as described in Appendix A of the PRE-TEST MOI, or equivalent, place the PUT in BISTFIS mode transmitting an HFTP pattern. Depending on the capability of the PUT, and the equipment available, it is acceptable to use either BIST-T or BIST-L to produce the needed test pattern.

If the PUT supports disconnects, remove the SATA PRE-TEST system, and connect SATA test fixture. Some PUTs require that the connection not be broken after BIST has been activated. In these situations, it may be necessary to use power splitters to allow simultaneous connection of the PRE-TEST system and the test equipment. Refer to Appendix A of the PRE-TEST MOI for additional details.

Start JIT3 application on Scope. Recall the setup: 'SATA jitter gen1' or 'SATA jitter gen1 ref wfm'. See Detailed Procedure in TSG-09 for additional information pertaining to TSG-10.

This test is only performed on Gen1 PUTs. Repeat PRE-TEST procedure and test using LBP. SSOP is optional. SSC is optional for this test.

Test pattern(s):	**SATA usage model:**
HFTP and LBP. SSOP is optional. (SSC optional)	1.5Gbps (Gen1i and Gen1m) PUTs that support 3Gbps should be tested at 1.5Gbps for this test

Gen1: 10 us/div, 50 ps/pt (> 100,000 UI)

Observable Results:

The DJ at Connector (Clock to Data, $f_{BAUD}/500$) value shall be less than 0.19 UI for 1.5Gbps PUTs.

Accuracy: estimated JNF is 2 ps rms

Possible Problems:
See LBP discussion in TSG-07 “Possible Problems” section.

Detailed Procedure:

Utilize the procedure described in TSG-09. The results for TSG-10 are available on the same display used to capture TSG-09 results. The following screen capture shows the location of the reading:

Test TSG-11 - TJ at Connector, Clock to Data, $f_{BAUD}/500$

Purpose: To verify that the TJ at Connector (Clock to Data, $f_{BAUD}/500$) of the PUT's transmitter is within the conformance limits.

References:

[1] SATA Standard, 7.2.1, Table 29 – Transmitted Signal Requirements
[2] Ibid, 7.2.2.3.12
[3] Ibid, 7.4.6, 7.4.8
[4] SATA unified test document, 2.12.11

Resource Requirements:

See appendix A.

Last Template Modification: May 15, 2006 (Version 1.0)

Discussion:

Reference [1] specifies the Transmitted Signal conformance limits for SATA PUTs. This specification includes conformance limits for the TJ at Connector (Clock to Data, $f_{BAUD}/500$). Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

Note: Prior to making this jitter measurement, it is necessary to follow the procedure in Appendix G, and determine the proper settings to use for Gen2 loop bandwidth in JIT3. The resulting loop bandwidth setting must be used for all Gen2 jitter measurements.

Test Setup:

Connect equipment as shown in Appendix B, figure 1 or 2 as appropriate. Note that it is acceptable to use either differential or pseudo-differential (single ended plus math waveform) probes for these measurements.

Test Procedure:

Using techniques and equipment as described in Appendix A of the PRE-TEST MOI, or equivalent, place the PUT in BISTFIS mode transmitting an HFTP pattern. Depending on the capability of the PUT, and the equipment available, it is acceptable to use either BIST-T or BIST-L to produce the needed test pattern.

If the PUT supports disconnects, remove the SATA PRE-TEST system, and connect SATA test fixture. Some PUTs require that the connection not be broken after BIST has been activated. In these situations, it may be necessary to use power splitters to allow simultaneous connection of the PRE-TEST system and the test equipment. Refer to Appendix A of the PRE-TEST MOI for additional details.

Start JIT3 application on Scope. Recall the setup: 'SATA jitter gen2' or 'SATA jitter gen2 ref wfm'. See the following detailed procedure for additional information.

This test is only performed on Gen2 PUTs. Repeat PRE-TEST procedure and test using LBP. SSOP is optional. SSC is optional for this test.

Test pattern(s):	**SATA usage model:**
HFTP and LBP. SSOP is optional (SSC optional)	3Gbps (Gen2i and Gen2m)

Gen2: 4 us/div, 25 ps/pt (> 100,000 UI)

Observable Results:

The TJ shall be less than 0.37UI when measured at $f_{BAUD}/500$ for 3.0Gbps PUTs.

Accuracy: estimated JNF is 2 ps rms

Possible Problems:
See LBP discussion under "Possible Problems" section of TSG-07.

Detailed Procedure:

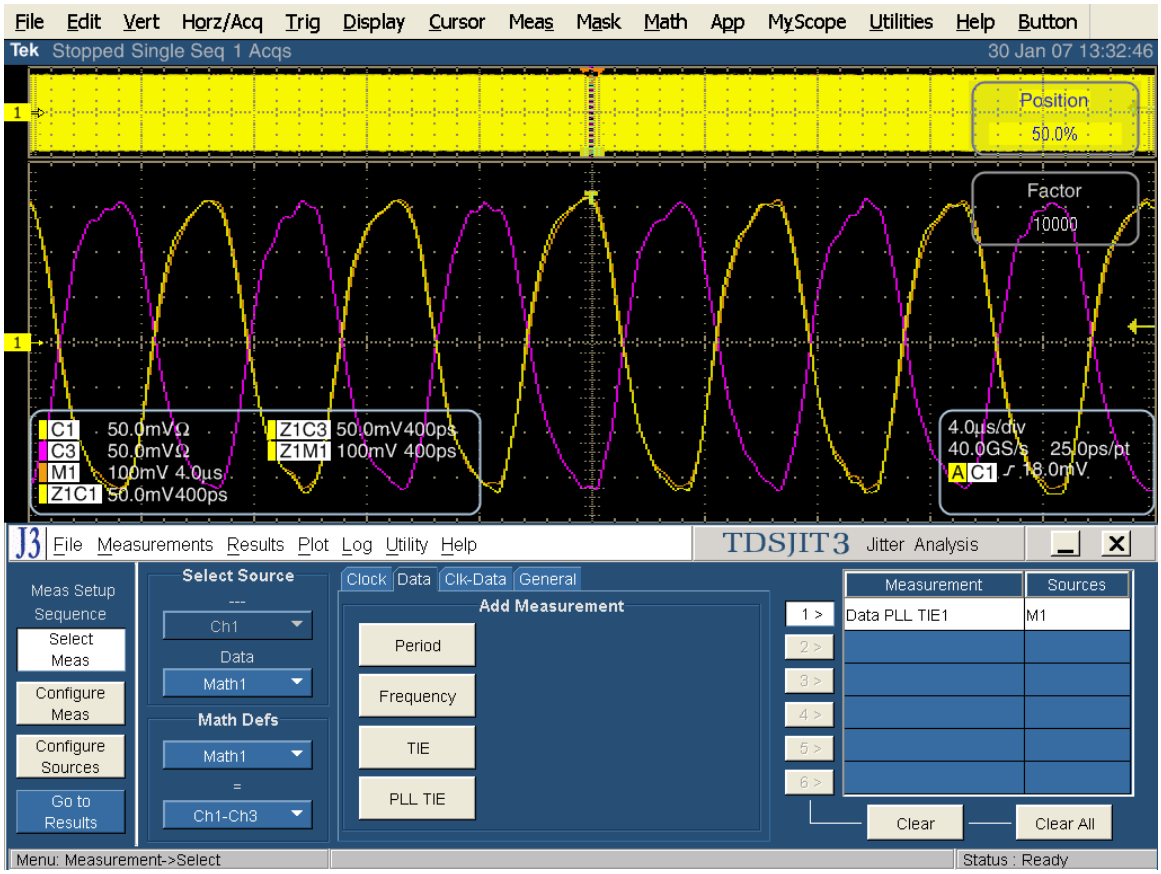
Scope setup: 4 us/div, 25 ps/pt. (Recall Instrument Setup from file 'SATA gen2 setup standard.set')

Run JIT3 version 2 by selecting App, Jitter Analysis – Advanced, from the Oscilloscope menu.

Cancel Jitter Wizard.

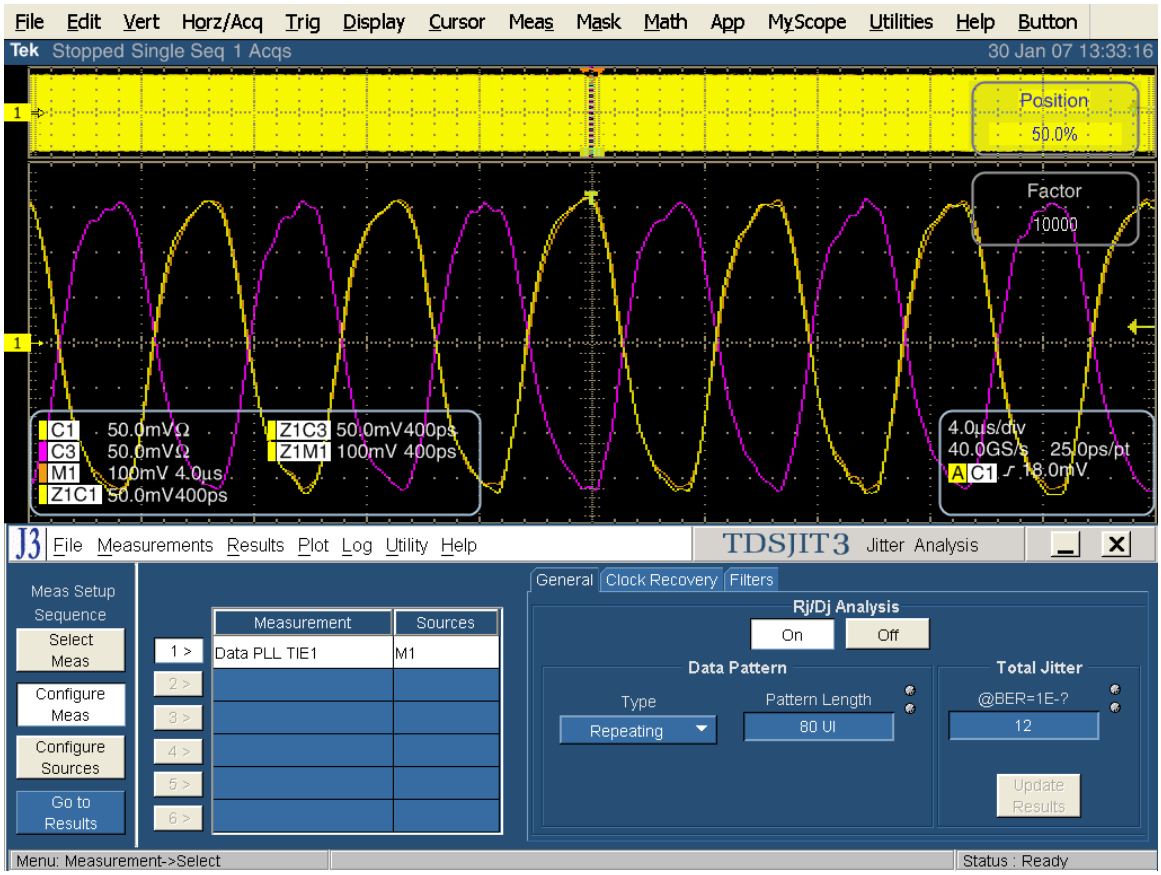
Define Data channel as Math1 = Ch1 – Ch3.

Select Data PLL-TIE (Source M1) from measurement menu.

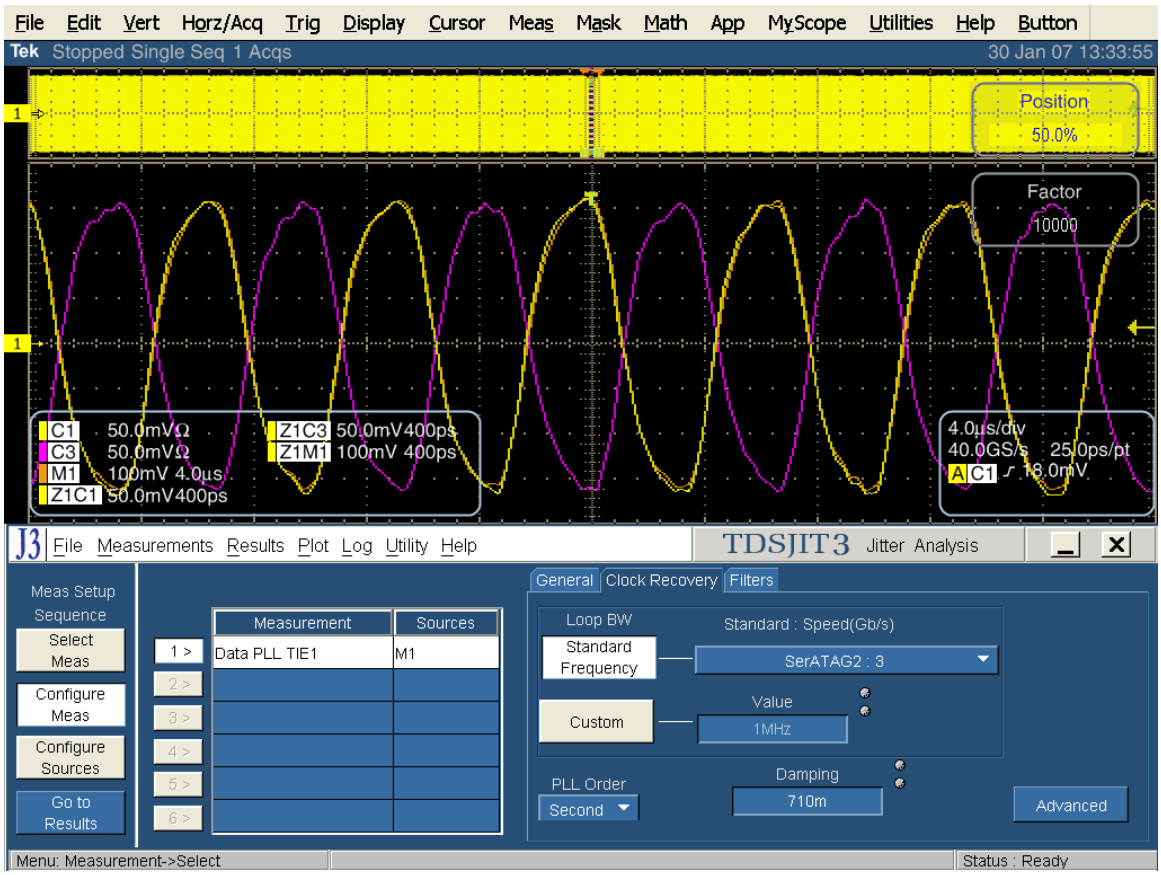


Configure measurement.

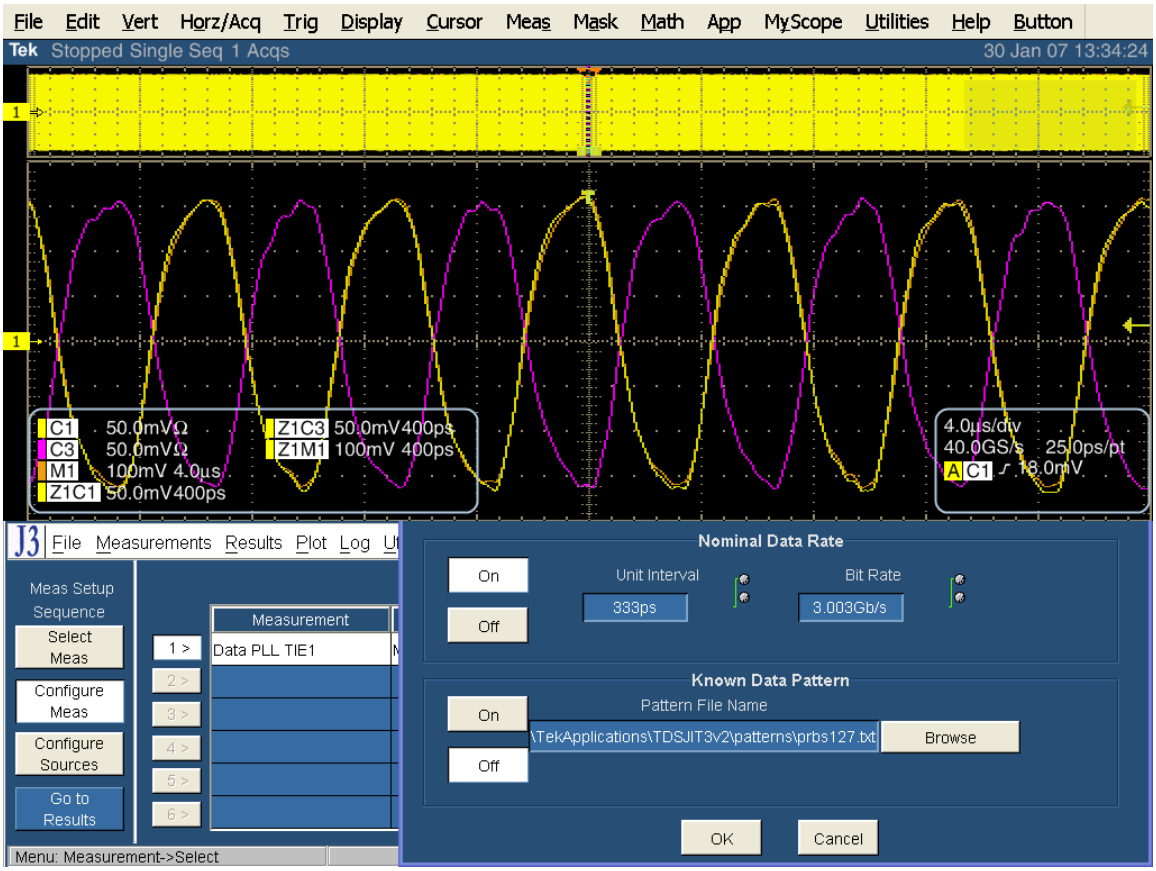
Select Repeating Rj/Dj separation, Pattern Length 80 UI, BER 1E-12.



Set ”PLL Order” to Custom (using loop bandwidth setting determined in procedure described in Appendix G) , second order PLL, with damping set to .710..

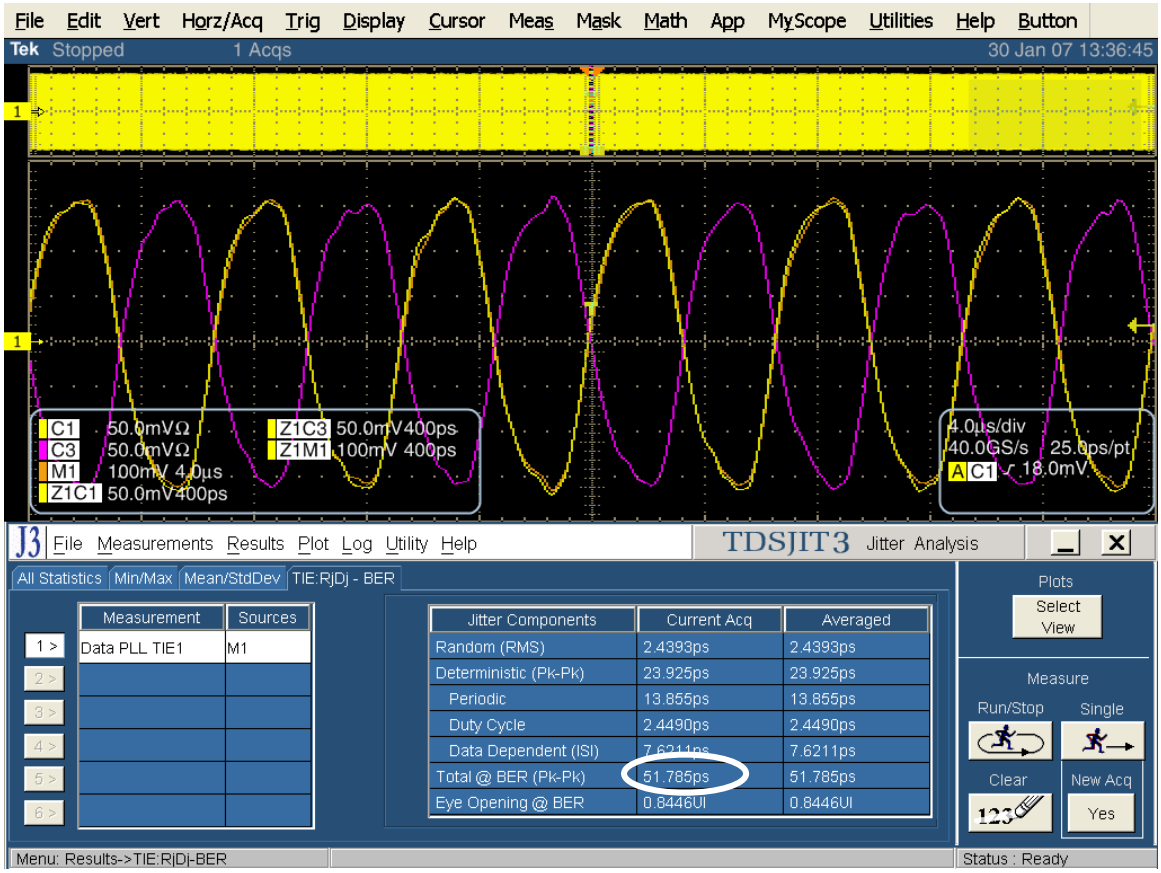


Set the nominal data rate at 3 Gbps under the advanced (clock recovery) button.



Then Go to results and press the Single button.

The Dj and Tj results will be under the TIE:RjDj – BER tab.



Test TSG-12 - DJ at Connector, Clock to Data, $f_{BAUD}/500$

Purpose: To verify that the DJ at Connector (Clock to Data, $f_{BAUD}/500$) of the PUT's transmitter is within the conformance limits.

References:

[1] SATA Standard, 7.2.1, Table 29 – Transmitted Signal Requirements
[2] Ibid, 7.2.2.3.12
[3] Ibid, 7.4.6, 7.4.8
[4] SATA unified test document, 2.12.12

Resource Requirements:

See appendix A.

Last Template Modification: May 15, 2006 (Version 1.0)

Discussion:

Reference [1] specifies the Transmitted Signal conformance limits for SATA PUTs. This specification includes conformance limits for the DJ at Connector (Clock to Data, $f_{BAUD}/500$). Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

Note: Prior to making this jitter measurement, it is necessary to follow the procedure in Appendix G, and determine the proper settings to use for Gen2 loop bandwidth in JIT3. The resulting loop bandwidth setting must be used for all Gen2 jitter measurements.

Test Setup:

Connect equipment as shown in Appendix B, figure 1 or 2 as appropriate. Note that it is acceptable to use either differential or pseudo-differential (single ended plus math waveform) probes for these measurements.

Test Procedure:

Using techniques and equipment as described in Appendix A of the PRE-TEST MOI, or equivalent, place the PUT in BISTFIS mode transmitting an HFTP pattern. Depending on the capability of the PUT, and the equipment available, it is acceptable to use either BIST-T or BIST-L to produce the needed test pattern.

If the PUT supports disconnects, remove the SATA PRE-TEST system, and connect SATA test fixture. Some PUTs require that the connection not be broken after BIST has been activated. In these situations, it may be necessary to use power splitters to allow simultaneous connection of the PRE-TEST system and the test equipment. Refer to Appendix A of the PRE-TEST MOI for additional details.

Start JIT3 application on Scope. Recall the setup: 'SATA jitter gen2' or 'SATA jitter gen2 ref wfm'. See the detailed procedure in TSG-11 for additional information related to TSG-12.

This test is only performed on Gen2 PUTs. Repeat PRE-TEST procedure and test using LBP. SSOP is optional. SSC is optional for this test.

Test pattern(s):	**SATA usage model:**
HFTP and LBP, (SSOP is optional) (SSC optional)	3Gbps (Gen2i and Gen2m)

Gen2: 4 us/div, 25 ps/pt (> 100,000 UI)

Observable Results:

The DJ shall be less than 0.19UI when measured at $f_{BAUD}/500$ for 3.0Gbps PUTs.

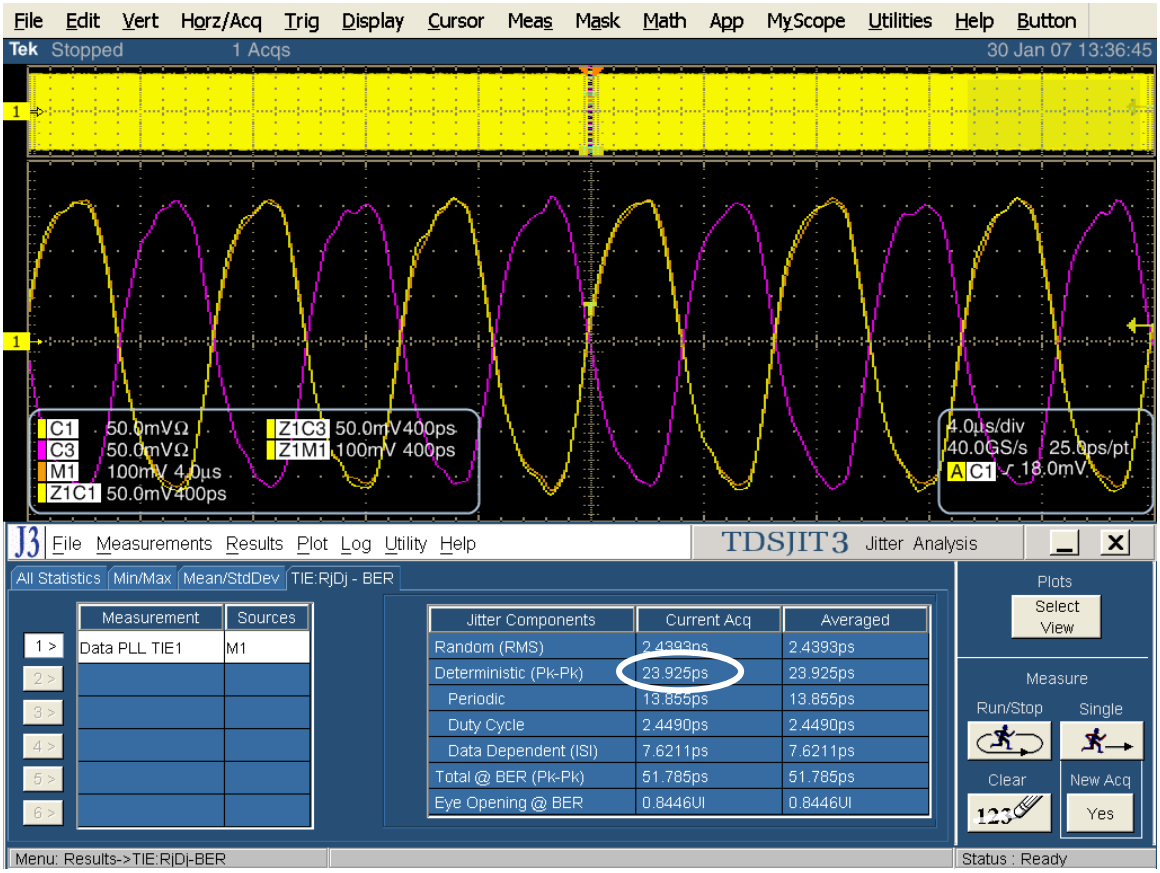
Accuracy: estimated JNF is 2 ps rms

Possible Problems:

See LBP discussion under “Possible Problems” section of TSG-07.

Detailed Procedure:

Utilize the procedure described in TSG-09. The results for TSG-10 are available on the same display used to capture TSG-09 results. The following screen capture shows the location of the reading:



PHY OOB REQUIREMENTS (OOB 1-7)

Overview:
This group of tests verifies the Phy OOB Requirements, as defined in Section 2.17 of the SATA Interoperability Unified Test Document, v1.3 (which references the SATA Standard, v2.6).

Test OOB-01 – OOB Signal Detection Threshold

Purpose: To verify that the OOB Signal Detection Threshold of the PUT's receiver is within the conformance limits.

References:

[1] SATA Standard, 7.2.1, Table 32 – OOB Specifications
[2] Ibid, 7.2.2.7.1
[3] Ibid, 7.4.20
[4] SATA unified test document, 2.14.1

Resource Requirements:

See appendix A.

See Appendix F for AWG7102 Amplitude Calibration procedure that is required to be performed prior to running the OOB-01 test.

Last Template Modification: May 15, 2006 (Version 1.0)

Discussion:

Reference [1] specifies the Transmitted Signal conformance limits for SATA PUTs. This specification includes conformance limits for the OOB Signal Detection Threshold. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

Test Setup:

Observe the setup outlined in Appendix C. If using the AWG7102, connect CH1 Analog outputs to PUT receiver inputs. Connect CH1 MKR1 to scope CH4. If using the AWG710, connect Marker 1 output to PUT Rx+, Marker 2 output to PUT Rx-, and Marker 2 BAR to scope CH4.

Set the scope to 200us/div, 1.25GS/s, and 800ps/pt. Set scope CH1 and CH3 to 50mV/div. Set Math waveform to Ch1-Ch3, and set math gain to 200mV/div. These settings can automatically be set by recalling the "SATA oob" setup file.

Connect scope CH1 and CH3 to the PUT Tx+ and Tx- respectively.

Test Procedure:

Note: The same test patterns are used to test both Gen1 and Gen2 PUTs. Per the SATA specification, the OOB signaling is performed only at 1.5Gbps. However, the SATA specification calls for different minimum amplitude for this test between Gen1 and Gen2 PUTs, as described in the following procedure.

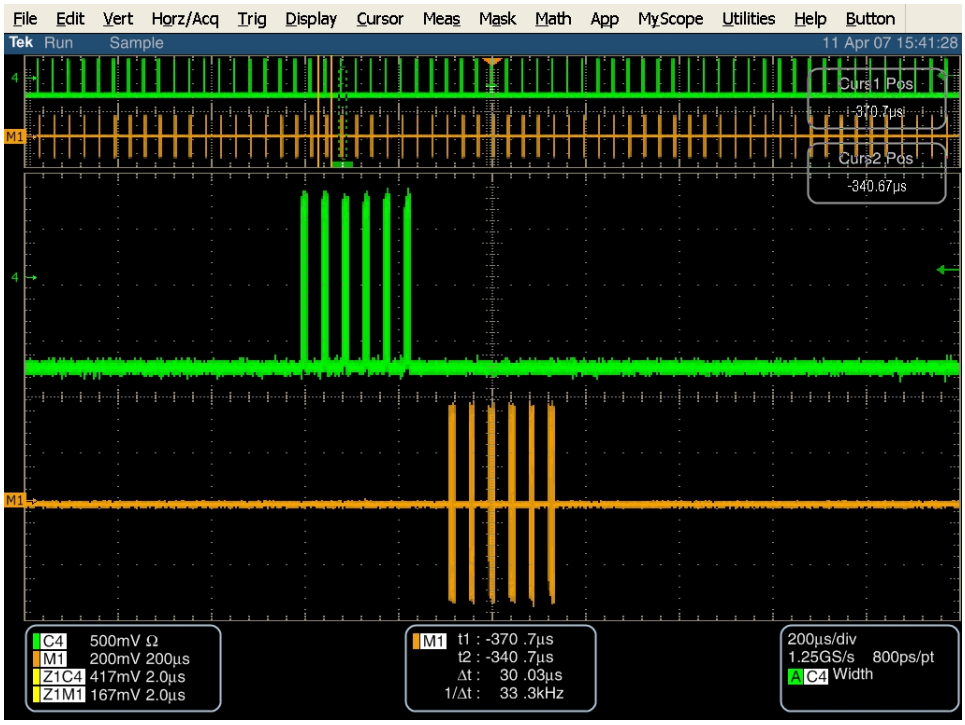
For PUTs running at both at 1.5Gbps and 3.0Gpbs, perform the following tests:

Load test pattern crst02-3G210.awg (compliance com-reset) on the AWG. This file sets the AWG to the required 210mV output amplitude using the COMRESET pattern.

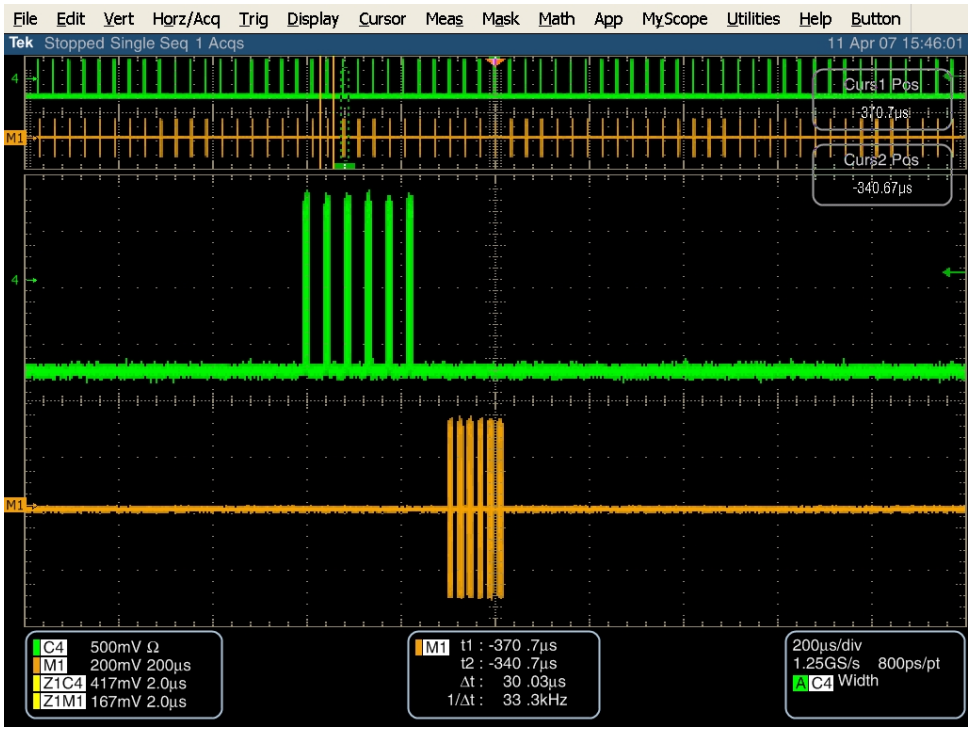
Verify that the PUT **provides** a stable response (valid detection) to the OOB signal from the AWG, as illustrated in the figures below.

There should be a response from the PUT to every COMINIT/COMRESET and COMWAKE pair from the AWG, across the entire 2ms acquisition. Any missing COMWAKEs will appear as gaps in the 2ms record, and should be considered a failure.

For Drive PUTs, a waveform similar to the following should be seen:



For HOST PUTs, a waveform similar to the following should be seen:



For Gen1 PUTS, load test pattern crst02-3G040.awg (compliance com-reset) on the AWG. For Gen2 PUTS, load test pattern crst02-3G060.awg (compliance com-reset) on the AWG. This file sets the AWG to the required 40mV or 60mV (1.5G or 3.0G spec limits) output amplitude using the COMRESET pattern. Verify that the PUT **does not provide** a response (no detection) to the OOB signal from the AWG, as illustrated in the figure below.

There should be NO response from the PUT to each COMINIT/COMRESET and COMWAKE pair from the AWG, across the entire 2ms acquisition. Any response will appear as signal in the 2ms math record, and should be considered a failure.

For both Drive and HOST PUTs, a waveform similar to the following should be seen:

Verify the OOB response according to the pass/fail criteria mentioned below.

Pass/Fail Criteria

- For PUTs running at 1.5Gbps:
  - Verification of PUT OOB detection at 210mV*
  - Verification of no PUT OOB detection at 40mV*
  - If any of the above cases fails, this is considered a failure by the PUT.
- For PUTs running at 3Gbps:
  - Verification of PUT OOB detection at 210mV*
  - Verification of no PUT OOB detection at 60mV*
  - If any of the above cases fails, this is considered a failure by the PUT.

Possible Problems:

Test OOB-02 – UI During OOB Signaling
Test OOB-03 – COMINIT/RESET and COMWAKE Transmit Burst Length
Test OOB-04 – COMINIT/RESET Transmit Gap Length
Test OOB-05 – COMWAKE Transmit Gap Length

Purpose: To verify that named parameters during OOB Signaling of the PUT's transmitter are within the conformance limits. Note. These measurements are combined into a MATLAB post processing analysis tool called SATAOOB.

References:

[1] SATA Standard, 7.2.1, Table 32 – OOB Specifications
[2] Ibid, 7.2.2.7.2
[3] Ibid, 7.4.11
[4] SATA unified test document, 2.14.2-5

Resource Requirements:

See appendix A.
SATAOOB.exe is available from ftp://ftp.tek.com/outgoing/SATAOOB_V1_3.zip

Note: Version 1.3 of the SATAOOB.exe meets the requirements of ECN #17. Please confirm that you are using version 1.3 of SATAOOB.exe for all SATA program revision 1.3 testing.

See Appendix C for non TDSRT-Eye setup details.

Last Template Modification: May 15, 2006 (Version 1.0)

Discussion:

Reference [1] specifies the Transmitted Signal conformance limits for SATA PUTs. This specification includes conformance limits for the UI During OOB Signaling. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

Test Setup:

Observe the setup outlined in Appendix C. Connect CH1 Analog outputs to PUT receiver inputs. Connect CH1 MKR1 to scope CH4.

Connect scope CH1 and CH3 to the PUT Tx+ and Tx- respectively.

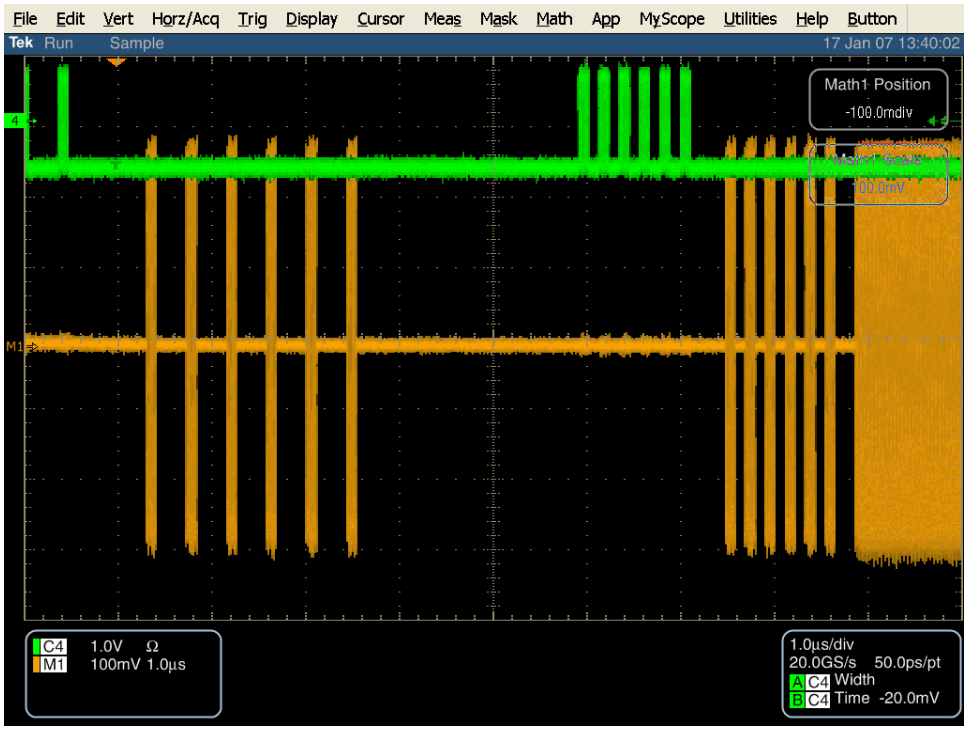
Load test pattern crst01-3G.AWG (compliance com-reset) on the AWG.

Test Procedure:

The following procedure is run once at the maximum interface rate for the PUT (1.5Gbps or 3Gbps).

1) Recall scope setup file "SATA OOB Timing Setup Normal.set".
2) Ensure proper test setup and AWG connections (Test Connection)
3) The setup creates MATH1 as CH1-CH3.
4) Acquire one waveform using Single Acq.
5) Save the MATH1 as wfm file in the test results folder
6) Run sataoob.exe utility to determine the OOB-related timing measurements. The utility will automatically detect the bursts in the waveform and determine burst and gap length.

For a Device, the acquired waveform should be similar to the display shown below. It may be necessary to adjust the time/div setting to acquire both the COMINIT and COMWAKE portions of the waveform. Make sure to keep the sample rate consistent while adjusting the time/div.

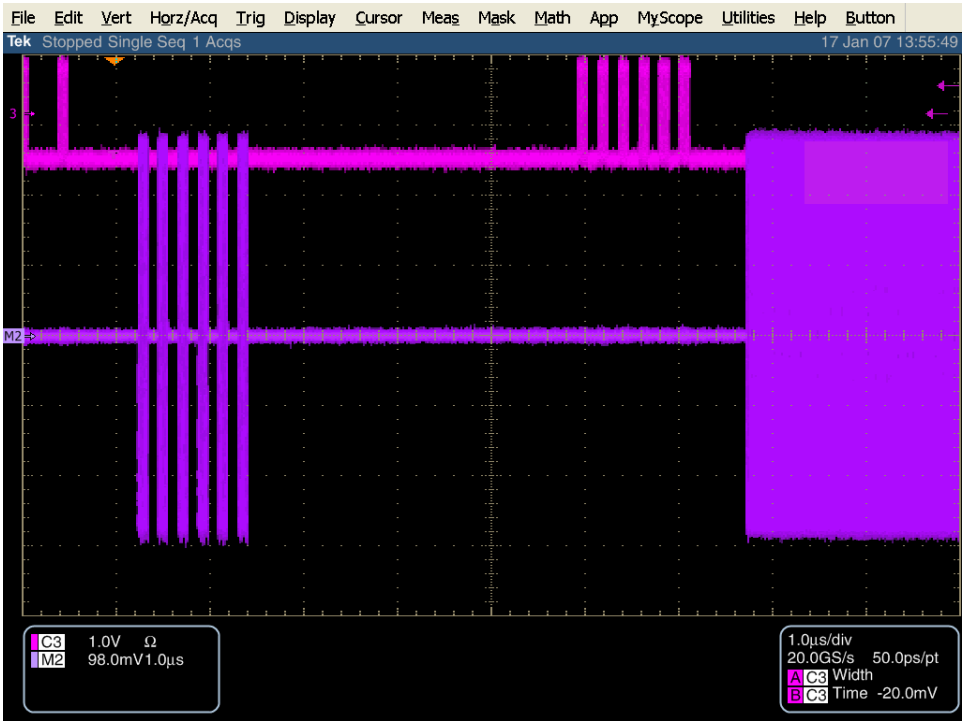


An example output of the utility after processing the Device waveform with the sataoob.exe utility follows:

```
*****************************************************
* SATA OOB Measurement 17-Jan-2007 16:33:10         *
* Tektronix, Inc 2006, Version 1.2 12/07/2006    *
*****************************************************

SATA OOB waveform detected with 12 bursts and 12 gaps
including COMINIT/RESET, COMWAKE and long gap between

UI during OOB Signaling
Average 654.03 ps

Transmit Burst Length: COMINIT/RESET and COMWAKE
Average 107.22 ns
Average 163.94 UI

COMINIT/RESET: Transmit Gap Length (5 gaps)
Average 319.45 ns
Average 488.44 UI

COMWAKE: Transmit Gap Length (5 gaps)
Average 106.06 ns
Average 162.17 UI
```

Hosts respond to the COMINIT/COMWAKE from the generator by sending out only a COMWAKE. Because of this, it is necessary to make two acquisitions for Hosts.

For the first Host acquisition, load the crst02-3G.awg test pattern into the AWG (compliance com-reset). The first acquired Host waveform (COMWAKE bursts) should be similar to the display shown below.

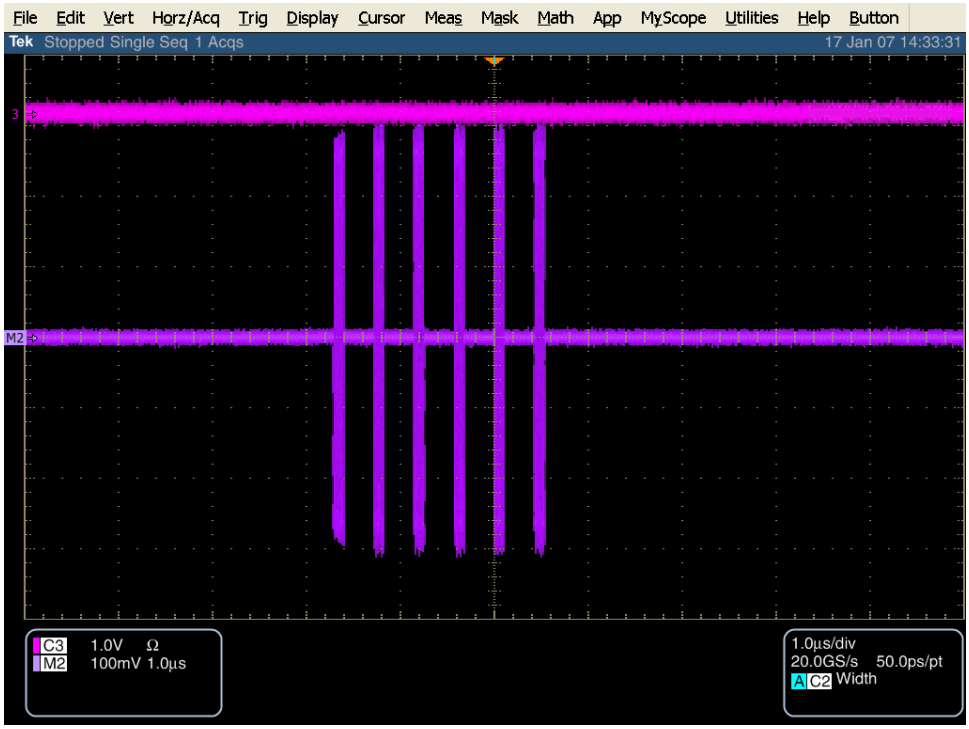


An example output of the measurement results after processing the first Host waveform with the sataoob.exe utility follows:

```
*****************************************************
* SATA OOB Measurement 17-Jan-2007 16:29:49         *
* Tektronix, Inc 2006, Version 1.2 12/07/2006    *
*****************************************************

SATA OOB waveform detected with 6 bursts and 6 gaps
appearing to be COMWAKE and long gap after

UI during OOB Signaling
Average 666.89 ps

Transmit Burst Length: COMWAKE
Average 107.85 ns
Average 161.73 UI

COMINIT/RESET: No bursts captured

COMWAKE: Transmit Gap Length (5 gaps)
Average 105.46 ns
Average 158.14 UI
```

Note that no COMINIT/RESET bursts were found in the previous waveform. It is necessary to capture the COMRESET from the Host in a separate acquisition. The COMRESET burst is transmitted automatically when the system is booting, so the easiest way to capture this is to arm the scope for a single acquisition, then boot the Host. Some hosts also asynchronously send out COMRESET bursts, and in this case it is not necessary to reboot the Host.

The second acquired Host waveform (COMRESET bursts) should be similar to the display shown below.



An example output of the measurement results after processing the second Host waveform with the sataoob.exe utility follows:

```
*****************************************************
* SATA OOB Measurement 17-Jan-2007 16:28:50         *
* Tektronix, Inc 2006, Version 1.2 12/07/2006    *
*****************************************************

SATA OOB waveform detected with 6 bursts and 5 gaps
appearing to be COMINIT/RESET

UI during OOB Signaling
Average 667.72 ps

Transmit Burst Length: COMINIT/RESET
Average 107.10 ns
Average 160.39 UI

COMINIT/RESET: Transmit Gap Length (5 gaps)
Average 320.30 ns
Average 479.69 UI

COMWAKE: No bursts captured
```

The final step in processing Host OOB measurements is to average the UI measurements for the COMWAKE and COMRESET acquisitions, and to average the Transmit Burst Length measurements for the COMWAKE and COMRESET acquisitions.

Observable Results:

Test OOB-02: The UI During OOB Signaling value shall be between 646.67 and 686.67ps.
Test OOB-03: COMINIT/RESET and COMWAKE Transmit Burst shall be between 103.5ns and 109.9ns.
Test OOB-04: COMINIT/RESET Transmit Gap shall be between 310.4ns and 329.6ns.
Test OOB-05: COMWAKE Transmit Gap Length shall be between 103.5ns and 109.9ns.

If measurements are within specified range, they have passed. Otherwise, they have failed.

Possible Problems:

Differential or pseudo-differential signals (e.g. MATH1=CH1-CH3) are recommend for this test to avoid noise problems. If the signal is noisy, or has a lot of crosstalk from adjacent traffic, the utility may have difficulty detecting the idle sections properly.

Some devices have a larger gap between the COMINIT and COMWAKE bursts. It is necessary to make sure that the acquired waveform contains both the COMINIT/RESET and COMWAKE bursts. Otherwise, the utility will not be able to make the measurements. Make sure that the waveform is captured properly. Another scope setup file is available for working with devices with larger gaps. The file is called “SATA OOB Timing Setup Long.set”. Otherwise, it may be necessary to manually increase the time/div setting on the scope to properly acquire the entire OOB sequence.

Test OOB-06 – COMWAKE Gap Detection Windows

Purpose: To verify that the COMWAKE Gap Detection Windows of the PUT's receiver are within the conformance limits.

References:

[1] SATA Standard, 7.2.1, Table 32 – OOB Specifications
[2] Ibid, 7.2.2.7.6
[3] Ibid, 7.4.21
[4] SATA unified test document, 2.14.6

Resource Requirements:

See appendix A,C

Last Template Modification: May 15, 2006 (Version 1.0)

Discussion:

Reference [1] specifies the Transmitted Signal conformance limits for SATA PUTs. This specification includes conformance limits for the COMWAKE Gap Detection Windows. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

Test Setup:

Observe the setup outlined in Appendix C. Connect CH1 Analog outputs to PUT receiver inputs. Connect AWG CH1 MKR1 to scope CH4.

Connect scope CH1 and CH3 to the PUT Tx+ and Tx- respectively. Set scope horizontal settings to 200us/div, 1.25GS/s, and 800ps/pt, Set math (Ch1-Ch3) to 200mV/div. The "SATA oob" settings file can be recalled to quickly put the scope into the desired state.

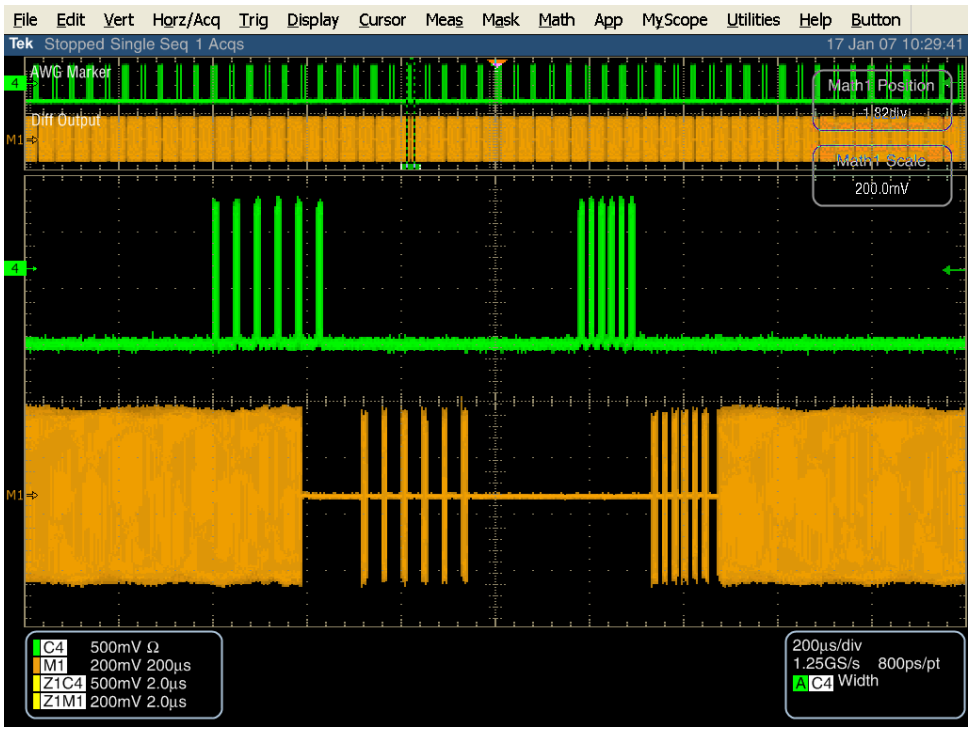
Test Procedure:

This test is run once at the maximum interface rate of the PUT (1.5Gbps or 3Gbps).

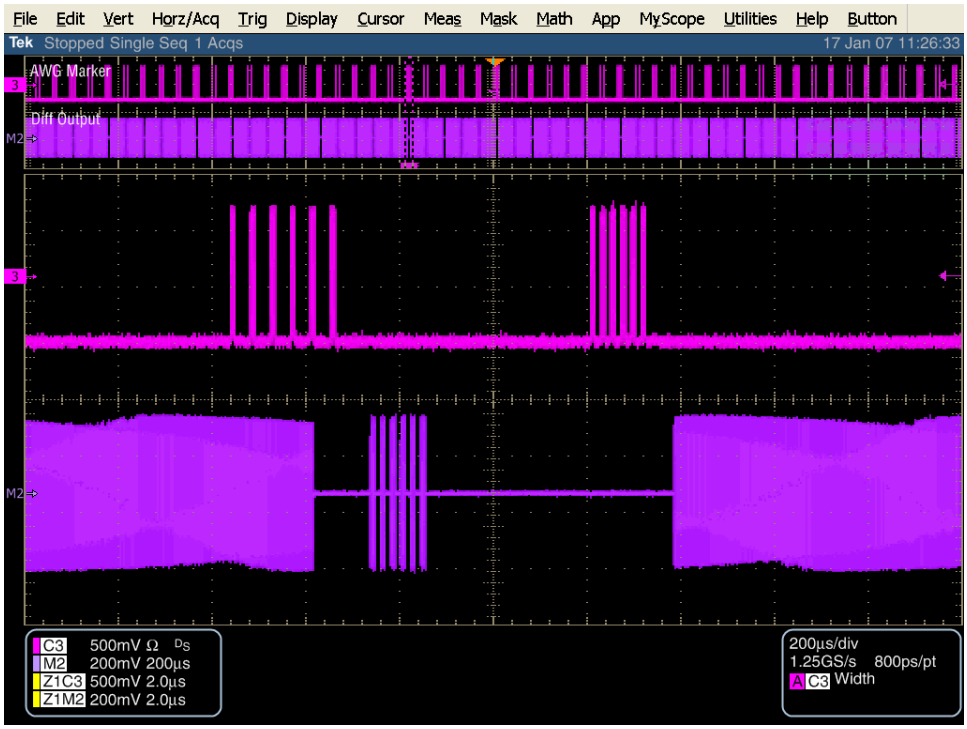
Load the cwke02-3G.awg file into the AWG7102. All of the AWG settings will be made automatically once the file is loaded. This will verify the OOB operation with 110nS comwake burst gap.

At this setting, the PUT should respond normally to the OOB sequence. There should be a response from the PUT to every COMWAKE, across the entire 2ms acquisition. Any missing COMWAKEs will appear as gaps in the 2ms record, and should be considered a failure.

For Drive PUTs, a waveform similar to the following should be seen:



For HOST PUTs, a waveform similar to the following should be seen:



Load the cwke03-3G.awg file into the AWG7102. All of the AWG settings will be made automatically once the file is loaded. This will verify the OOB operation with 103nS comwake burst gap.

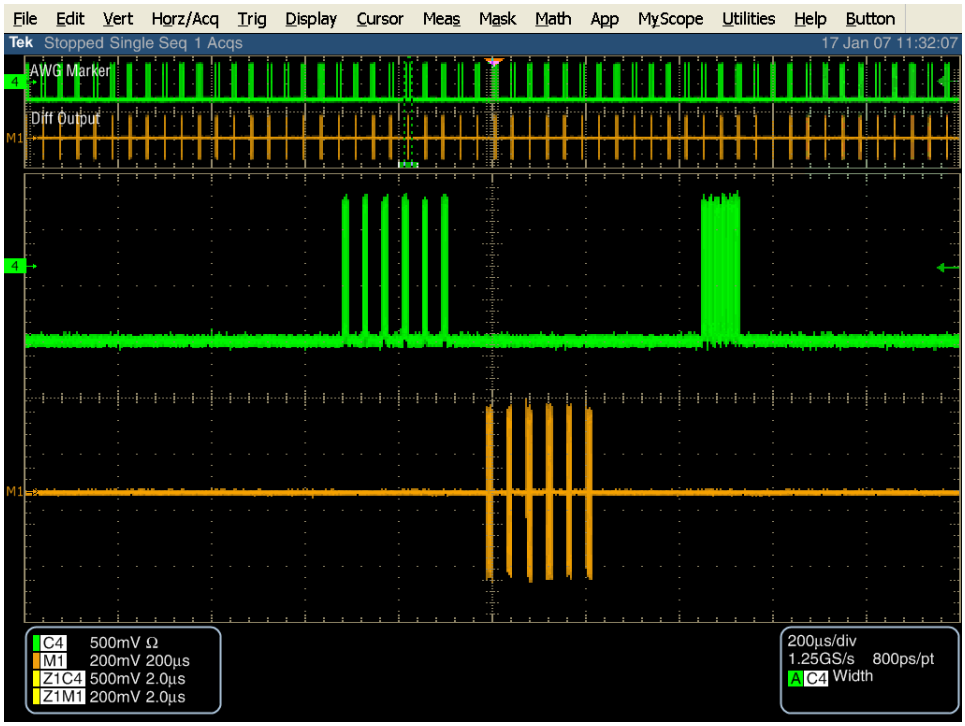
At this setting, the PUT should respond normally to the OOB sequence. Again, there should be a response from the PUT to every COMWAKE, across the entire 2ms acquisition. Any missing COMWAKEs will appear as gaps in the 2ms record, and should be considered a failure.

For Drive and Host PUTs, the acquired waveforms should be similar to those shown when running the cwke02-3G.awg file described above.

Load the cwke04-3G.awg file into the AWG7102. All of the AWG settings will be made automatically once the file is loaded. This will verify the OOB operation with 177nS comwake burst gap.

At this setting, the PUT should not respond to the OOB sequence. There should be no response from the PUT across the entire 2ms acquisition, other than the COMINIT/COMRESET bursts. Any response, other than the COMINIT/COMRESET, across the entire 2ms record should be considered a failure.

For both Drive and HOST PUTs, a waveform similar to the following should be seen:



Load the cwke05-3G.awg file into the AWG7102. All of the AWG settings will be made automatically once the file is loaded. This will verify the OOB operation with 30nS comwake burst gap.

At this setting, the PUT should not respond to the OOB sequence. There should be no response from the PUT across the entire 2ms acquisition, other than the COMINIT/COMRESET bursts. Any response, other than the COMINIT/COMRESET, across the entire 2ms record should be considered a failure.

For both Drive and HOST PUTs, a waveform similar to the waveform shown for the cwke04-3G.awg test should be seen.

Possible Problems:

In-Spec Observable Results:

The PUT shall respond to COMWAKE at the lower limit of 103ns.
The PUT shall respond to COMWAKE at the upper limit of 110ns.

Out-of-Spec Observable Results:

The PUT shall not respond to COMWAKE at the lower limit of 30ns.
The PUT shall not respond to COMWAKE at the upper limit of 177ns.

Test OOB-07 – COMINIT Gap Detection Windows

Purpose: To verify that the COMINIT Gap Detection Windows of the PUT's receiver are within the conformance limits.

References:

[1] SATA Standard, 7.2.1, Table 32 – OOB Specifications
[2] Ibid, 7.2.2.7.7
[3] Ibid, 7.4.21
[4] SATA unified test document, 2.14.7

Resource Requirements:

See appendix A, C

Last Template Modification: April 12, 2006 (Version 1.0)

Discussion:

Reference [1] specifies the Transmitted Signal conformance limits for SATA PUTs. This specification includes conformance limits for the COMINIT Gap Detection Windows. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

Test Setup:

Observe the setup outlined in Appendix C. Connect CH1 Analog outputs to PUT receiver inputs. Connect CH1 MKR1 to scope CH4.

Connect scope CH1 and CH3 to the PUT Tx+ and Tx- respectively.

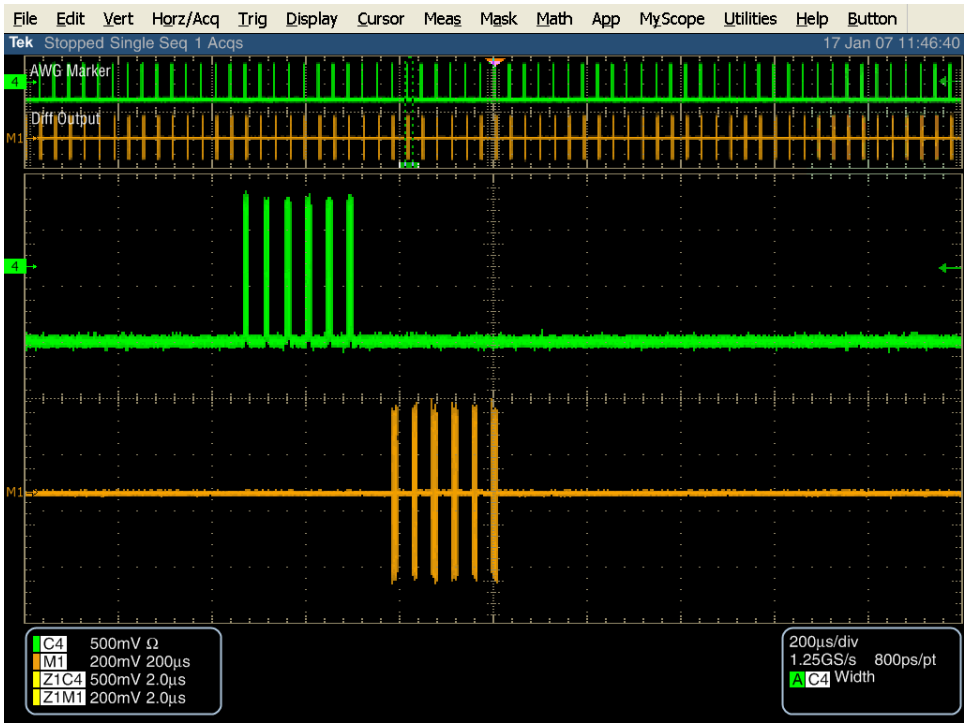
Test Procedure:

This test is run once at the maximum interface rate of the PUT (1.5Gbps or 3Gbps).

Load the crst02-3G.awg file into the AWG7102. All of the AWG settings will be made automatically once the file is loaded. This will verify the OOB operation with 334nS COMRESET/COMINIT burst gap.

At this setting, the PUT should respond normally to the OOB sequence.

For both Drive and Host PUTs, a waveform similar to the following should be seen:



Load the crst03-3G.awg file into the AWG. All of the AWG settings will be made automatically once the file is loaded. This will verify the OOB operation with 306nS COMRESET/COMINIT burst gap.

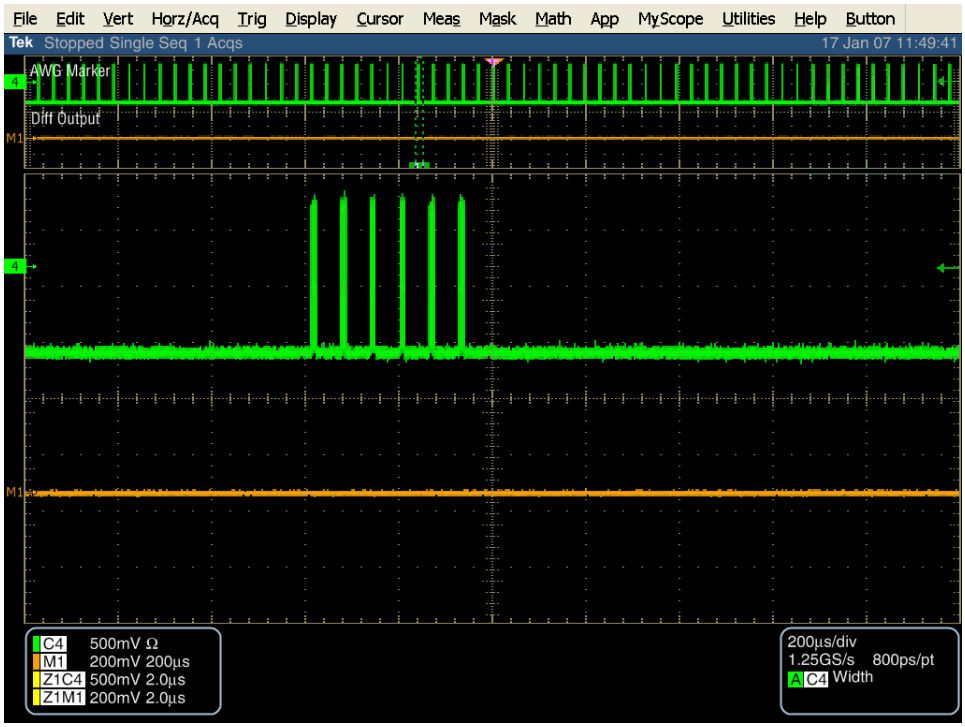
At this setting, the PUT should respond normally to the OOB sequence.

For Drive and Host PUTs, the acquired waveforms should be similar to those shown when running the crst02-3G.awg file described above.

Load the crst04-3G.awg file into the AWG. All of the AWG settings will be made automatically once the file is loaded. This will verify the OOB operation with 527nS COMRESET/COMINIT burst gap.

At this setting, the PUT should NOT respond to the OOB sequence.

For both Drive and Host PUTs, a waveform similar to the following should be seen:



Load the crst05-3G.awg file into the AWG. All of the AWG settings will be made automatically once the file is loaded. This will verify the OOB operation with 173nS COMRESET/COMINIT burst gap.

At this setting, the PUT should not respond to the OOB sequence.

For Drive and Host PUTs, the acquired waveforms should be similar to those shown when running the crst04-3G.awg file described above.

Inter Burst Observable Results:

The PUT shall respond with COMINIT at the lower limit of 306ns.
The PUT shall respond with COMINIT at the upper limit of 334ns.

Out-of-Spec Observable Results:

The PUT shall not respond with COMINIT at the lower limit of 173ns.
The PUT shall not respond with COMINIT at the upper limit of 527ns.

Possible Problems:

The effective detection of out-of-spec behavior can be problematic, particularly when measured on an Oscilloscope. The Instrument is set to single sequence (1 shot trigger) on the first incidence of any traffic from the PUT. Observations have been made which show the PUT responding to the *FIRST* COMRESET issued by the AWG regardless of its burst properties. The subsequent pulses show no response from the PUT however, which is the spec compliant behavior.

A PUT my take up to 10ms to respond to the received COMRESET. It is necessary to make sure that the PUT is responding/not responding (as expected) by viewing up to 11ms after the COMRESET. It may be necessary to manually adjust the scope for a larger time/div setting to inspect this 10ms window.

Note: If the PUT supports Asynchronous Signal Recovery, it can pro-actively transmit a COMINIT which is not in direct response to receiving a COMRESET. During testing, it is essential to ignore any COMINIT which is a result of Asynchronous Signal Recovery, and only test COMINIT responses that are a result of receiving a COMRESET from the AWG.

Appendix A – Resource Requirements

The resource requirements include two separate sets of equipment. The equipment required for PHY and TSG tests is shown in section A.1, and the equipment required for TX and RX tests is shown in section A.2, and the equipment required for OOB tests is shown in section A.3.

A.1 Equipment for PHY and TSG tests

1. Real-time Digital Oscilloscope
   DPO/DSA72004, DPO/DSA 71604, DPO/DSA 71254, TDS6154C, TDS612C

   For Gen1-only testing, the following scopes are also acceptable:
   DPO/DSA 70804 or TDS6804B (These are not acceptable for Gen2 Compliance Test)

2. Test Fixture
   Crescent Heart Software Fixture TF-SATA-NE/XP, TF-SATA-FE/XP
   Or equivalent

3. Cables
   174-4944-00 or equivalent

4. PRE-TEST system
   Any system capable of placing the PUT in BIST mode, and producing the desired test pattern.

5. Software
   PRE-TEST utility as required
   Tektronix TDSJIT3v2 (version 3.0.1 or later)
   Tektronix TDSRT-Eye (RTeye version 3.0.2 or later, SST module version 3.0.2 build 9 or later)

A.2 Equipment for OOB tests

1. Real-time Digital Oscilloscope
   DPO/DSA72004, DPO/DSA 71604, DPO/DSA 71254, TDS6154C, TDS612C

   For Gen1-only testing, the following scopes are also acceptable:
   DPO/DSA 70804 or TDS6804B (These are not acceptable for Gen2 Compliance Test)

2. Signal Generator
   AWG7102, AWG710B, or AWG710
   Test Fixture
   Crescent Heart Software Fixture TF-SATA-NE/XP, TF-SATA-FE/XP
   Or equivalent

3. Cables
   174-4944-00 or equivalent

4. SATA PRE-TEST System
   Any system capable of placing the PUT in BIST mode, and producing the desired test pattern.

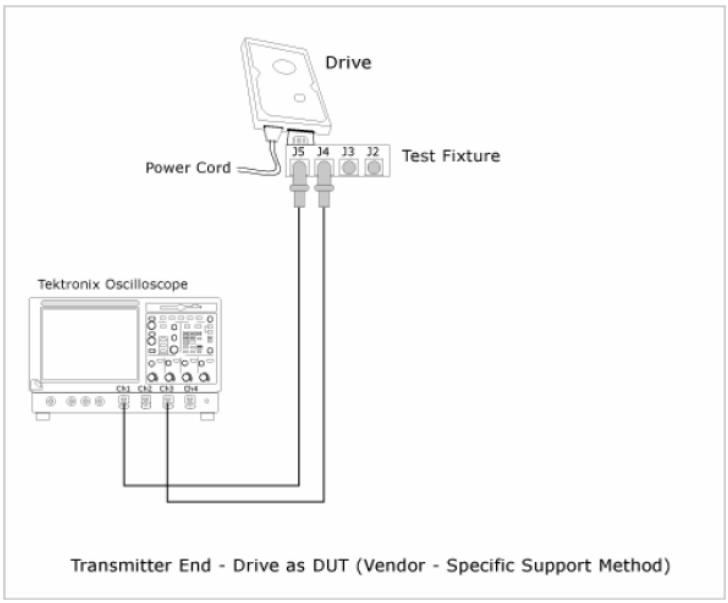
5. Software

PRE-TEST utility as required
AWG pattern/sequence files
Tektronix TDSJIT3v2 (version 3.0.1 or later)
Tektronix TDSRT-Eye (RTeye version 3.0.2 or later, SST module version 3.0.2 build 9 or later)
SATA OOB Utility (version 1.2 or later)

Appendix B – Test Setups

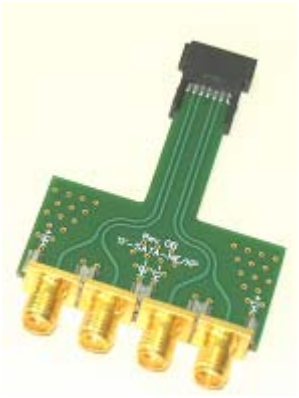
Transmitter Device PUT tests using BIST-FIS

Once the Device or Drive PUT has been put in BIST-FIS mode and is generating the appropriate test pattern the following configuration should be made.

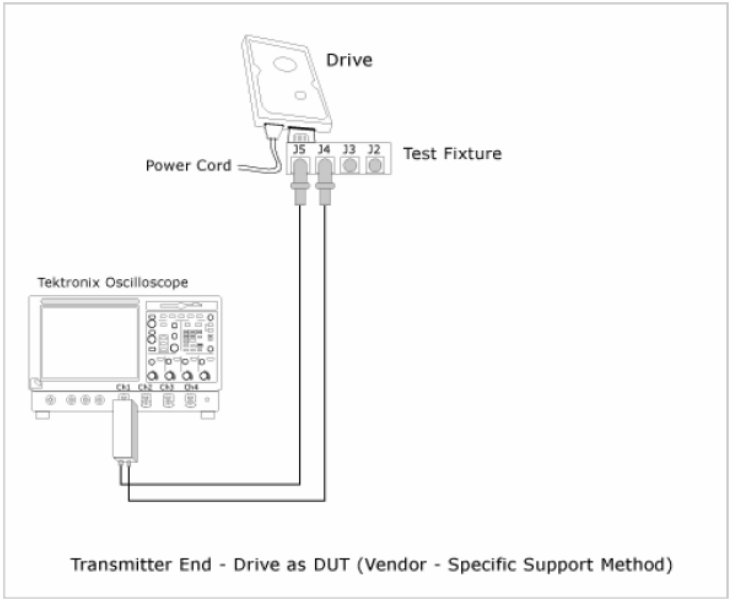


A - Setup with SMA cables

Fixture Pinout Info
For DRIVE connection



J2	J3	J4	J5
Rx+	Rx-	Tx-	Tx+
S2	S3	S5	S6

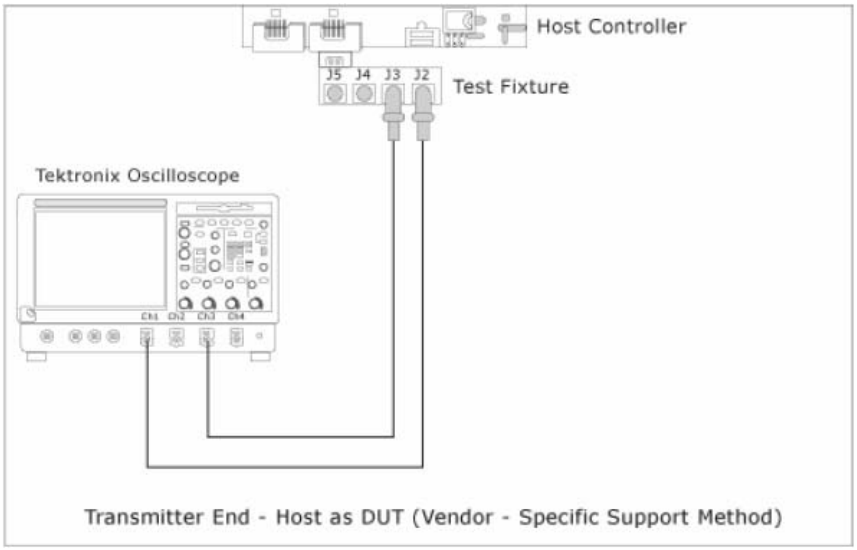


B - Setup with differential probe

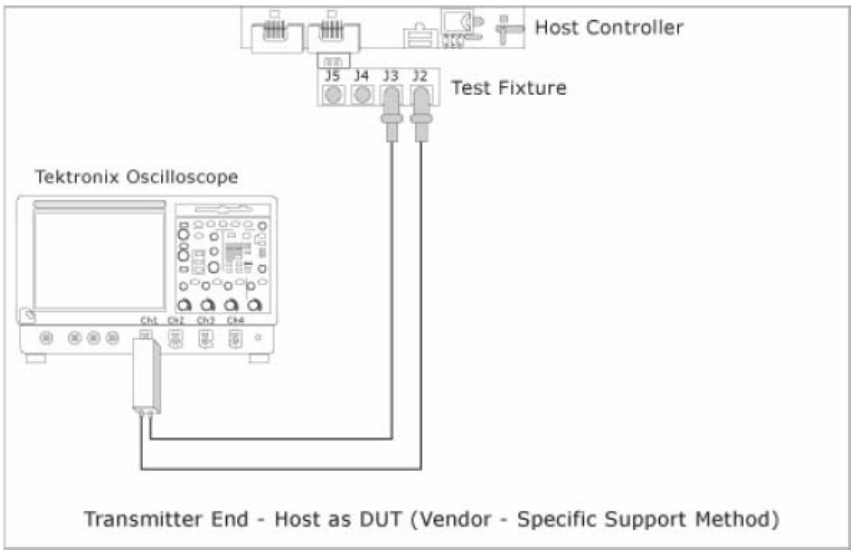
Figure 1: Test the transmitter drive PUT using BIST FIS/User method

Transmitter Host PUT tests using BIST-FIS

Once the Host PUT has been put in BIST-FIS mode and is generating the appropriate test pattern the following configuration should be made.

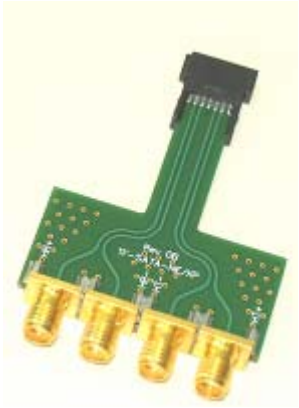


A - Setup with SMA cables



B - Setup with differential probe

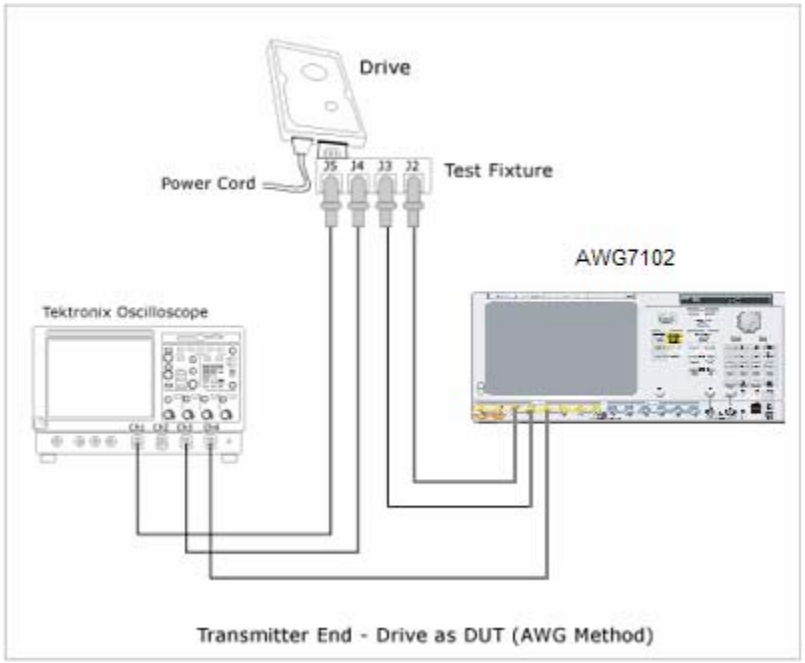
Fixture Pinout Info
For HOST connection



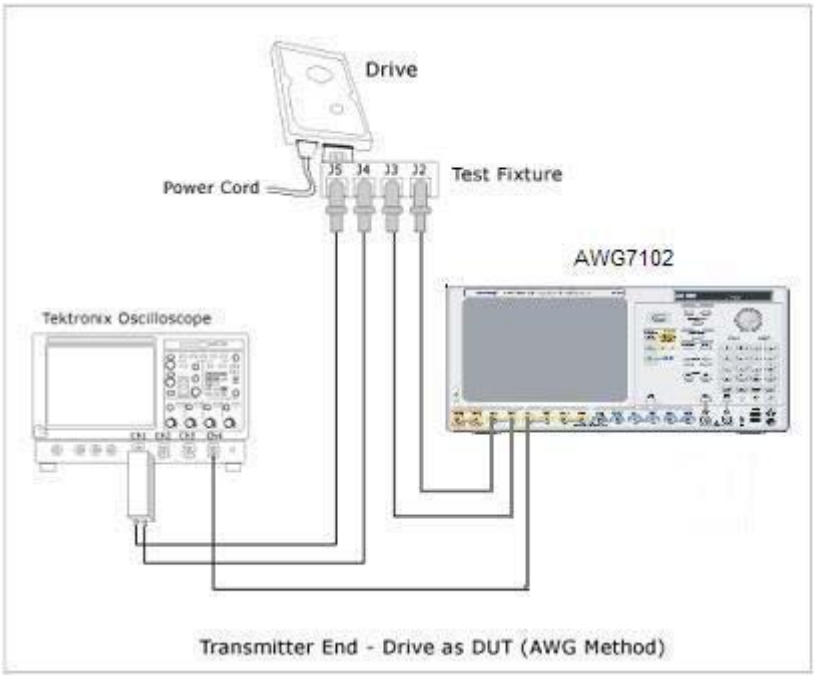
J2	J3	J4	J5
Tx+	Tx-	Rx-	Rx+
S2	S3	S5	S6

Figure 2: Test the transmitter host PUT using BIST FIS/User method

Out-of-band (OOB) Device PUT tests using AWG



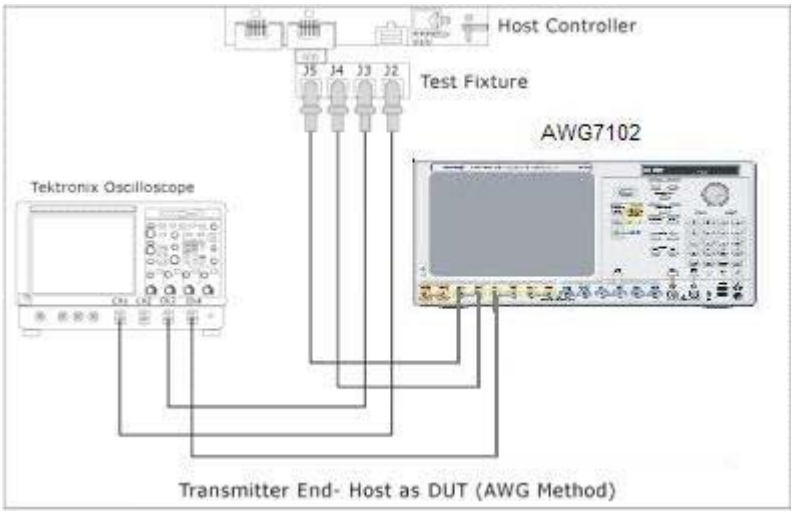
A - Setup with SMA cables



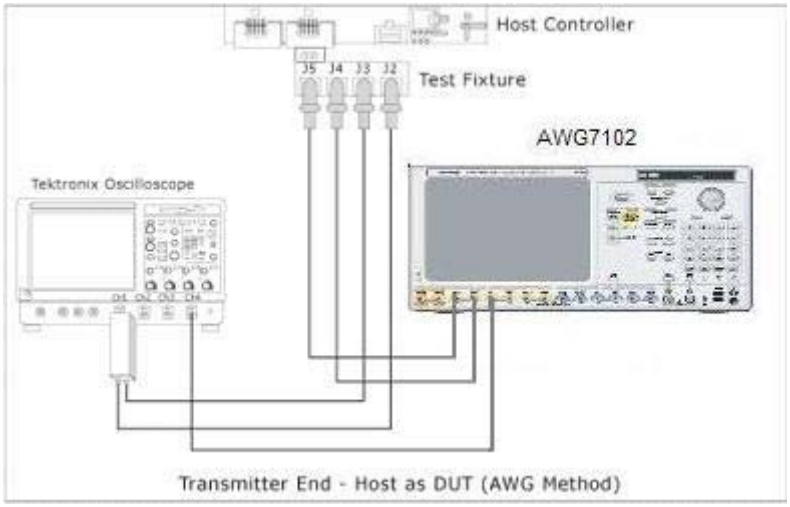
B - Setup with differential probe

Figure 3: OOB Drive test using AWG

Out-of-band (OOB) Host PUT tests using AWG



A - Setup with SMA cables



B - Setup with differential probe

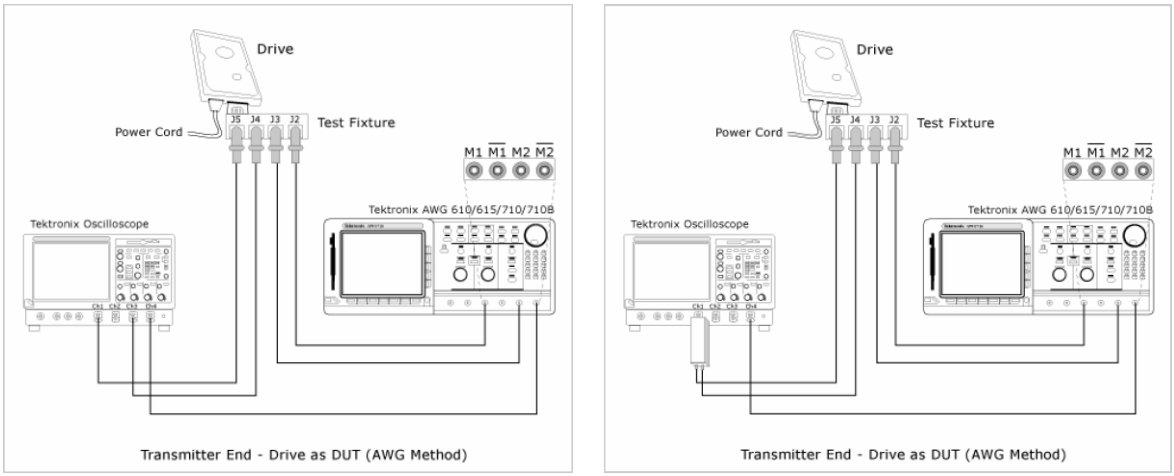
Figure 4: OOB Host test using AWG

Appendix C – OOB Setup Procedures

Procedure for obtaining the required OOB signals requires SATAOOB utility:

Depending on which of the following two configurations the user desires, follow setup procedure A or B as shown in Figure C.1.0.

Out-of-band (OOB) Device PUT tests using AWG

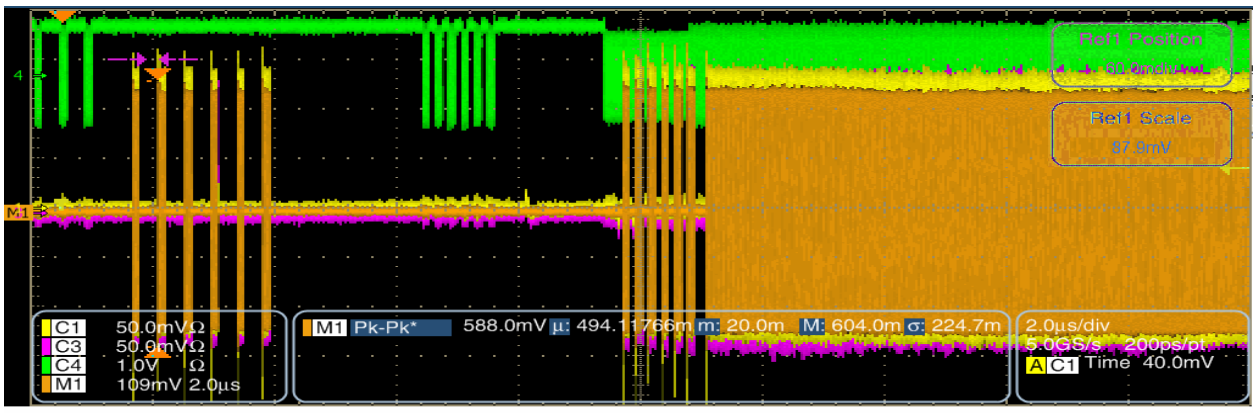


A - Setup with SMA cables

B - Setup with differential probe

Figure C.1.0: OOB Drive test using AWG

Setup a timeout trigger for 3.5µsec and a post trigger placement at roughly 10% of the acquisition as illustrated in the following screen shot of a proper OOB signal. In this illustration, Setup A was observed which requires setting up a math waveform of M1 = (CH1 – CH3). Save this resultant waveform to a Tektronix WFM file. This file will be fed into the SATAOOB utility.



Appendix D – Real-Time DSO Measurement Accuracy

Tables D.1 and D.2 outline the system and individual measurement accuracy parameters for the SATA measurements outlined in his MOI when performed on a Real Time Oscilloscope of 8 GHz Bandwidth or higher.

Table D.1 System specific performance parameters for SATA compliant instruments

Characteristics	Value
Bandwidth	20GHz (DPO/DSA 72004) 16GHz (DPO/DSA 71604) 15GHz (TDS6154C) 12.5GHz (DPO/DSA 71254) 12GHz (TDS6124C) 8GHz (DPO/DSA 70804, TDS6804B) (8GHz only useful for Gen1 PUT testing)

Table D.2 Measurement specific performance parameters for current IW SATA measurements.

Spec number	**Measurement**	**Accuracy**	**Notes:**
PHY-01	UI	3 ps rms	DTA expression
PHY-02	LT freq	+/-2 ppm	time base accuracy
PHY-03	SSC freq	+/-2 ppm	time base accuracy
PHY-04	SSC dev	+/-2 ppm	time base accuracy
TSG-01	DOV	typical noise 4 mV (@ 800 mV FS)	0.5 % rms
TSG-02	RFT	1.607086367	18 ps 20/80 risetime
TSG-03	Skew	3 ps rms	DTA expression + offset
TSG-04	AC CM V	typical noise <2 mV (@ 800 mV FS)	filter reduces vertical noise
TSG-05	RFI	< 1.6 % typical	risetime1 is 1.6% off, risetime2 is less than 1.6% off
TSG-06	Amp Imb	< 0.5 % rms	vertical noise is averaged
TSG-07	Tj	Estimated JNF is 2 ps rms	JNF expression
TSG-08	Dj	Estimated JNF is 2 ps rms	JNF expression
TSG-09	Tj	Estimated JNF is 2 ps rms	JNF expression
TSG-10	Dj	Estimated JNF is 2 ps rms	JNF expression
TSG-11	Tj	Estimated JNF is 2 ps rms	JNF expression
TSG-12	Dj	Estimated JNF is 2 ps rms	JNF expression

Appendix E – Return Loss Verification Procedure

This procedure outlines the use of a Time Domain Network Analyzer (TDNA) to measure/verify the Lab Load return loss. Since there is good correlation between return loss measurements made a TDNA and a Vector Network Analyzer (VNA), it is acceptable to make the measurement with either system.

The SATA specification requires that the Lab Load (scope input, including cables) have a return loss of -20dB or more up to 5GHz, and -10dB or more from 5GHz to 8GHz. The Tek scopes meet this requirement at all settings, except for the 50mV/div setting. At the 50mV/div setting, the use of an external 6dB attenuator allows meeting the specification, without significantly impacting the quality or integrity of the measurement. Empirical data has shown that the return loss performance does not substantially impact the measurement results; reliable measurements can be made for debug and diagnostic work without using external attenuators. However, it is necessary to add the external attenuation during the SATA Compliance Tests to assure meeting the SATA specification requirements for Lab Loads.

The return loss performance of the Lab Load (TDS scope) is stable over time. Perform this procedure once for each of the channels being used on the scope prior to an Interoperability Workshop/Compliance Test session to verify that the Lab Load meets the SATA specification requirements.

The Tek TDNA systems consists of the following equipment:
TDS8000, TDS8200, or CSA8200 equivalent time sampling scope
80E04 sampling module
Tek Iconnect TDNA software

To calibrate the measurements, a high quality 50 ohm SMA cable, and high quality 50 ohm calibration load is needed.

Detailed Procedure:
Turn on the power of the scope, and set the vertical sensitivity to 50mV/div for the channel being tested. All other settings for the scope do not effect the return loss. Install a TCA-SMA adapter, and connect a 6dB SMA attenuator to the TCA-SMA. Connect the SMA cable (the same cable that will be used for PUT testing) to the 6dB attenuator.

On the TDNA system, make the following settings:

Vert: 100mV/div
Position = 1 div
Offset = 250mV

Horiz: 2ns/div
Record length = 4000
Position approx. 35ns

ACQ: Average 128 samples
Set “Stop After” to Condition = Average Complete

Acquire Open Reference Trace

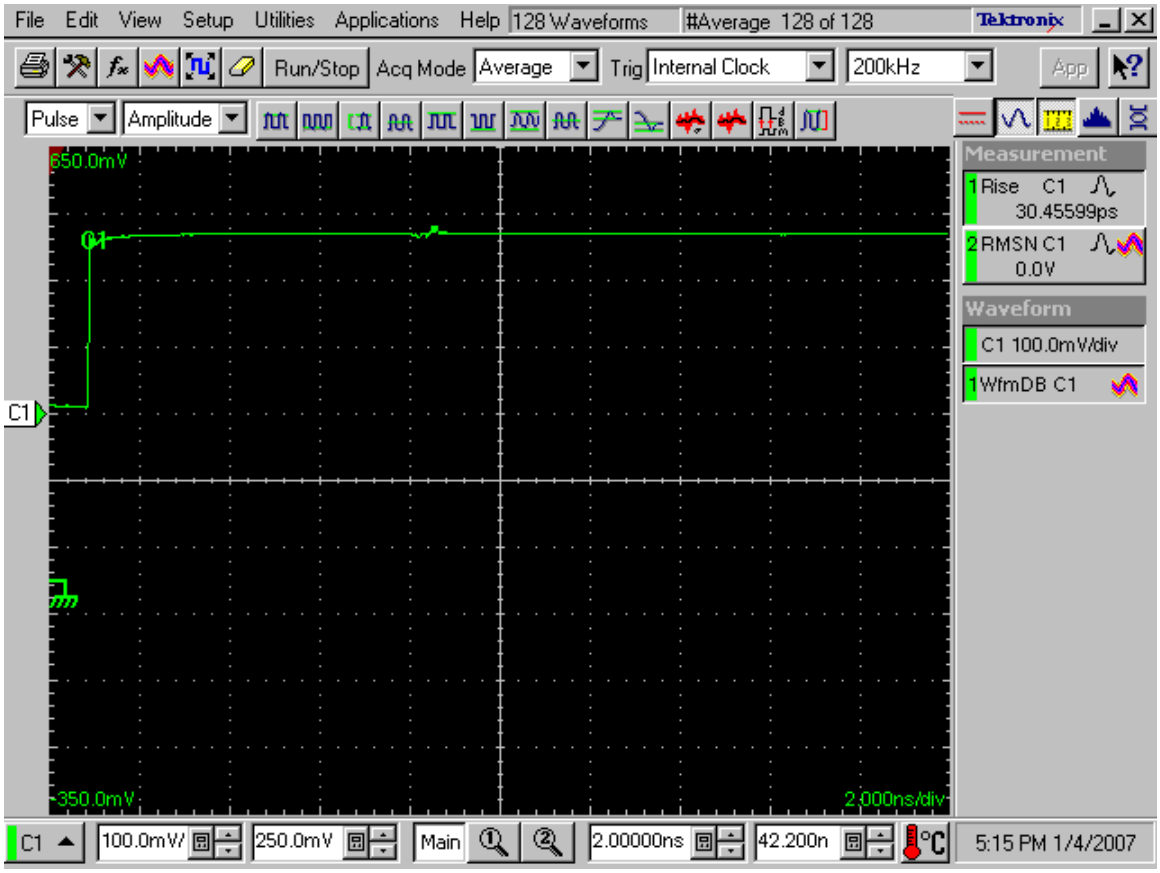
Using the TDNA scope setup controls, turn on TDR and ACQ (under the TDR setup tab).

It is necessary to adjust the horizontal position on the TDNA scope to move the incident pulse just off the left side of the display. When using the SMA connector on the 80E04 as the reference plane, it can be difficult to make this

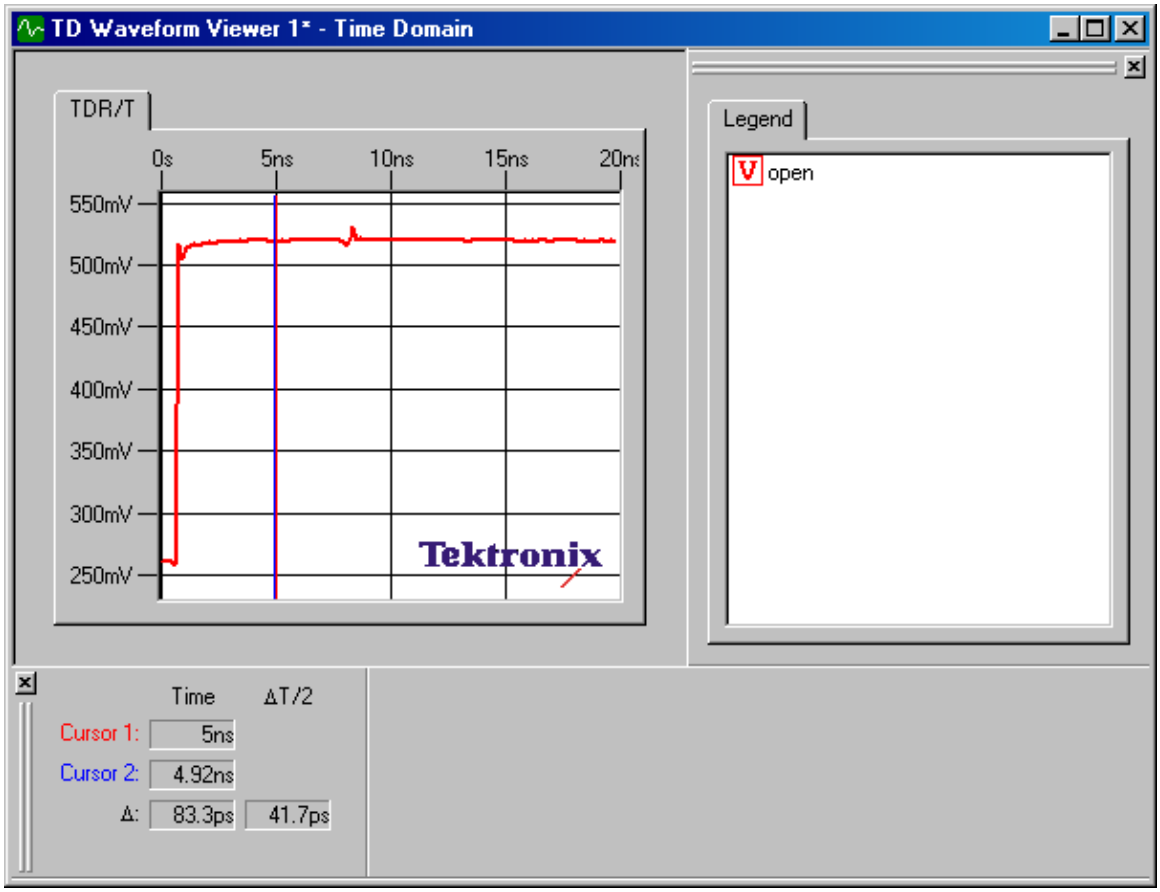
adjustment. By connecting a short, high quality SMA cable to the front of the 80E04, the reference plane can be defined as the far end of the cable (away from the 80E04 connection). In this case, there will be a much longer time from the incident pulse to the reflection, and the adjustment to move the incident pulse off the screen is much easier. Once this has been done, use this short cable for the entire return loss analysis; the end of this cable becomes the reference plane for measurement.

Remove all loads from the TDNA reference plane, and acquire an open waveform by pressing the Clear button on the front panel of the TDNA system, then pressing the Run button. Wait for the # Average count at the top right side of the scope display to show 128 of 128, indicating completion of the acquisition.

The results should be similar to the display below:



Go to the IConnect screen, and press the acquire button to transfer the waveform to the IConnect environment. Rename this waveform to something descriptive such as “open” by double clicking on the name, and editing. The result of this is shown below:


TD Waveform Viewer 1* - Time Domain
TDR/T
0s
5ns
10ns
15ns
20ns
550mV
500mV
450mV
400mV
350mV
300mV
250mV
Tektronix
Legend
open
Time
ΔT/2
Cursor 1:
5ns
Cursor 2:
4.92ns
Δ:
83.3ps
41.7ps

Acquire 50 ohm Reference Trace

Next, connect the high quality 50 ohm calibration load to the TDNA reference plane. Repeat the procedure described for acquiring the open waveform to acquire the 50 ohm waveform.

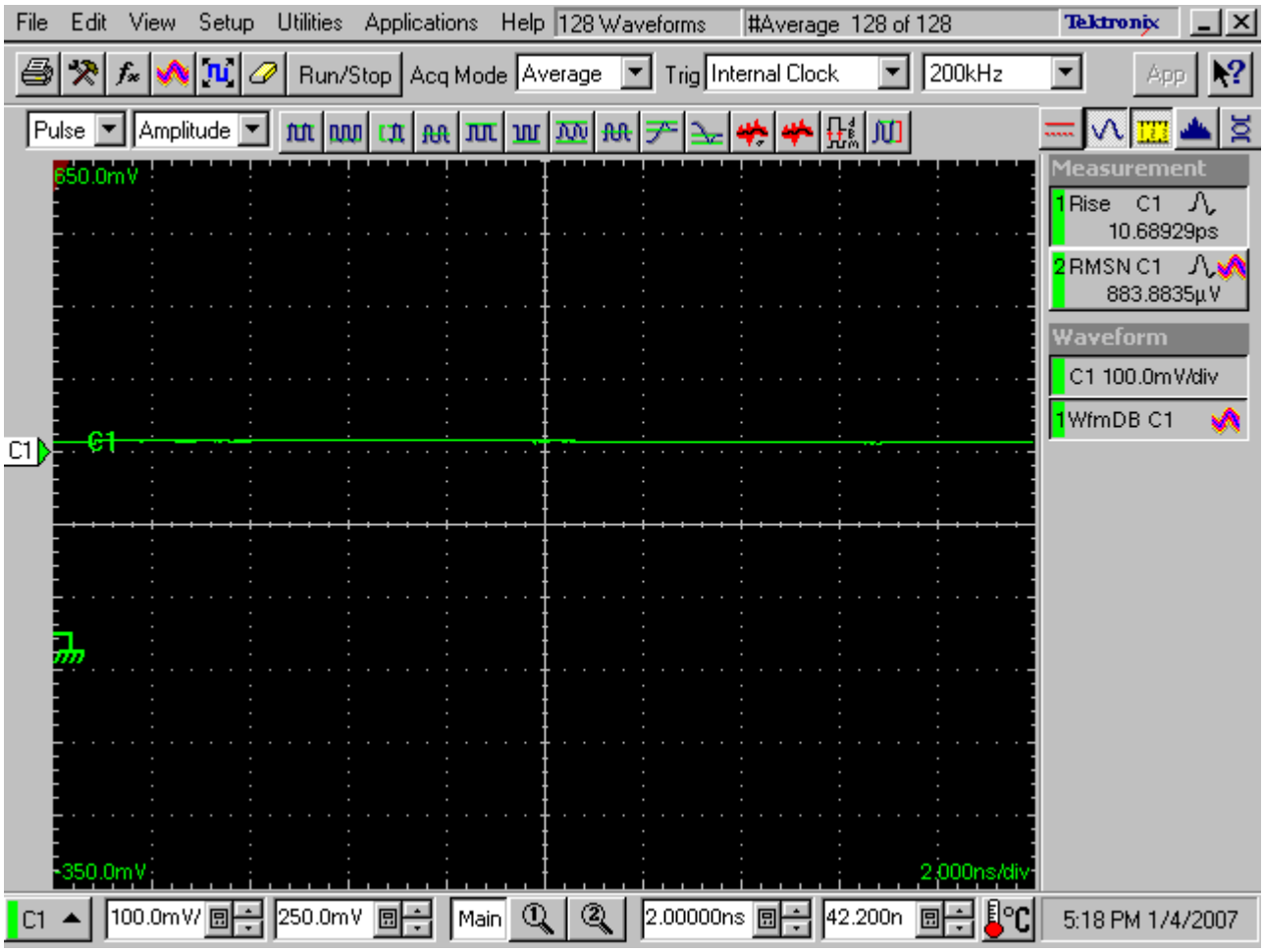
The results should be similar to the display below:

Repeat the process of acquiring the waveform in IConnect, as described above, and rename the waveform to something descriptive such as “50ohm”.

Acquire TDS6124C/TDS6154 Channel Trace

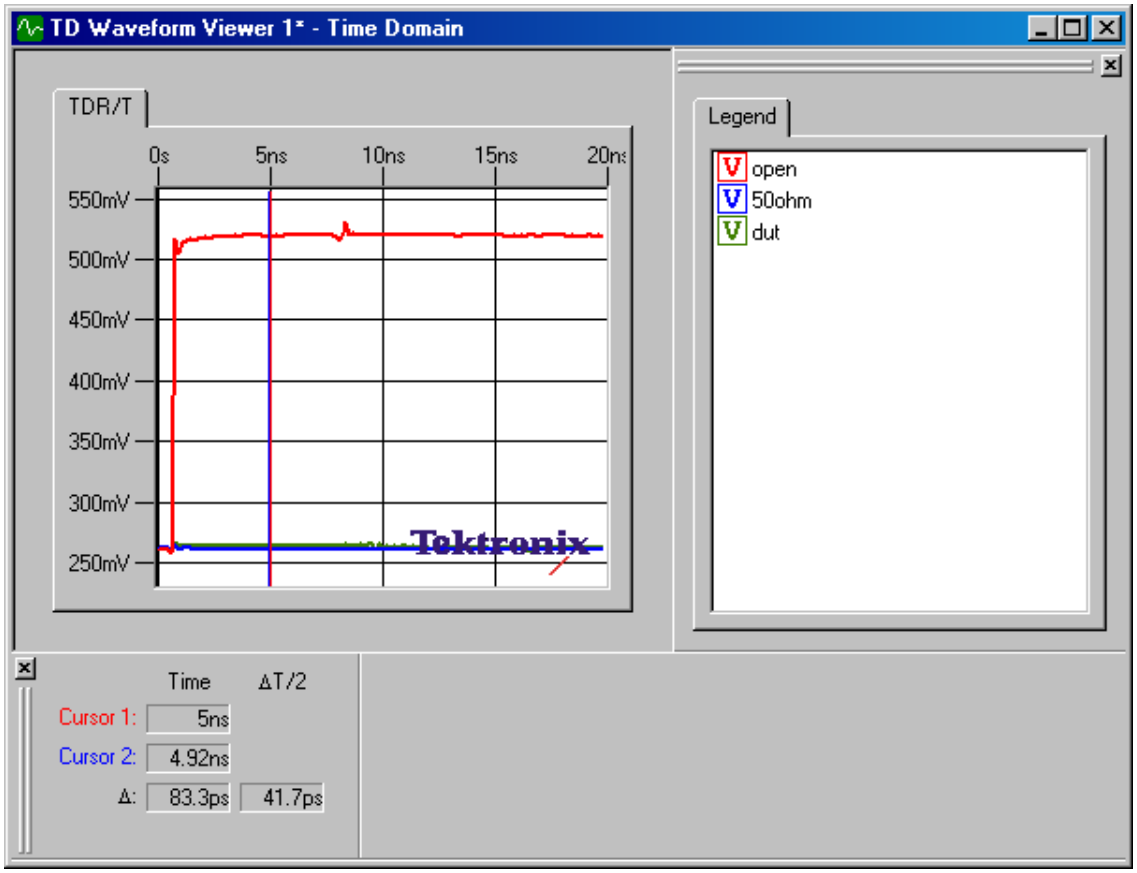
Connect the scope lab load (full channel including scope, TCA-SMA, 6dB attenuator, and the SMA cable that will be used for SATA testing) to the TDNA reference plane. Repeat the process described for the Open reference waveform to acquire the Lab Load waveform.

The results should be similar to the display below:



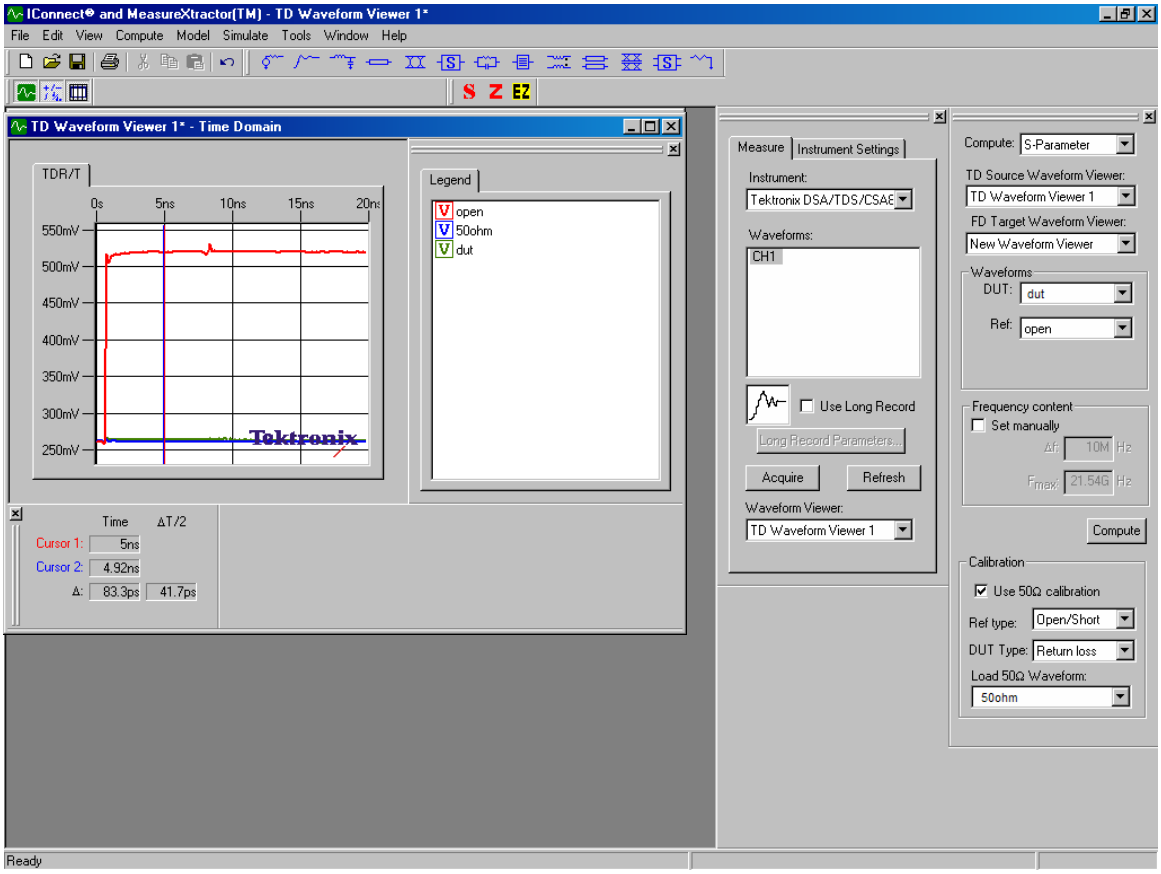
As in the previous steps, go to the IConnect screen, and press acquire to transfer the waveform to IConnect. Once complete, rename the waveform to something descriptive such as “dut”.

At this point, all the raw data has been collected to generate the return loss plot. The Waveform Viewer in the IConnect display should look like:

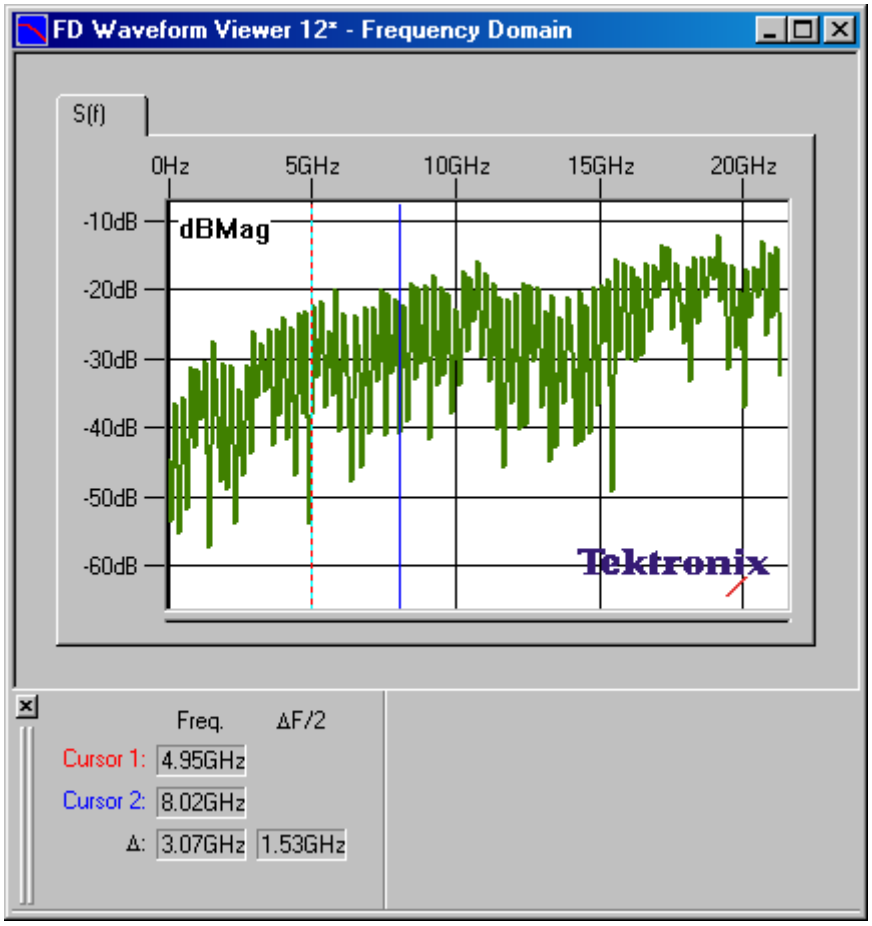


Running the Return Loss Analysis

Once the waveforms have been acquired, press the “Compute” button in IConnect.



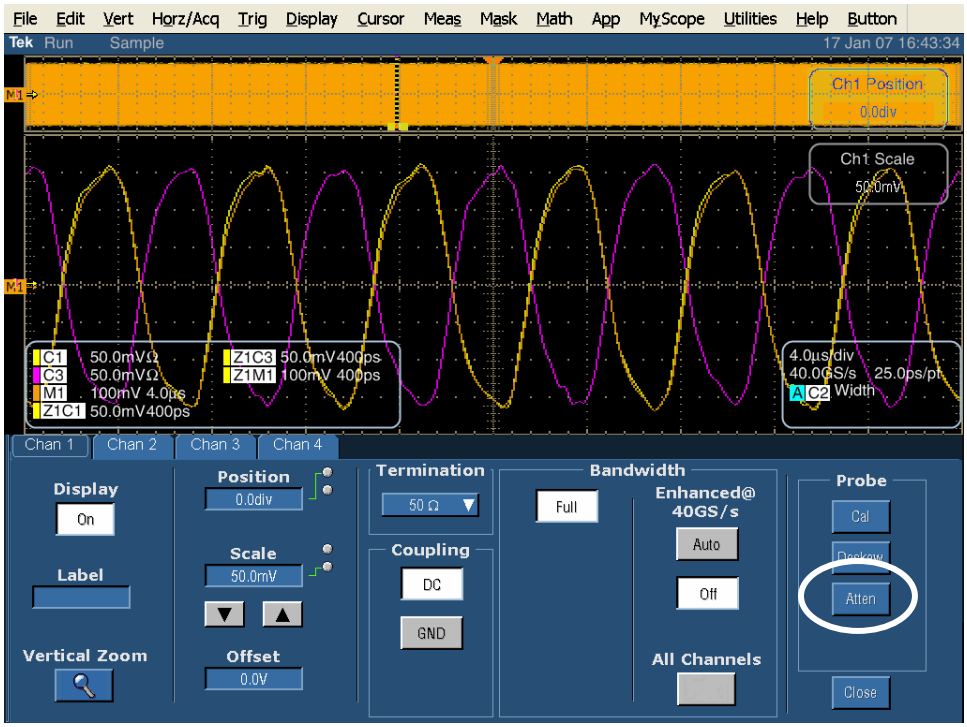
When the analysis is complete, a new window will open automatically with the resulting return loss plot. An example of the result is shown below.



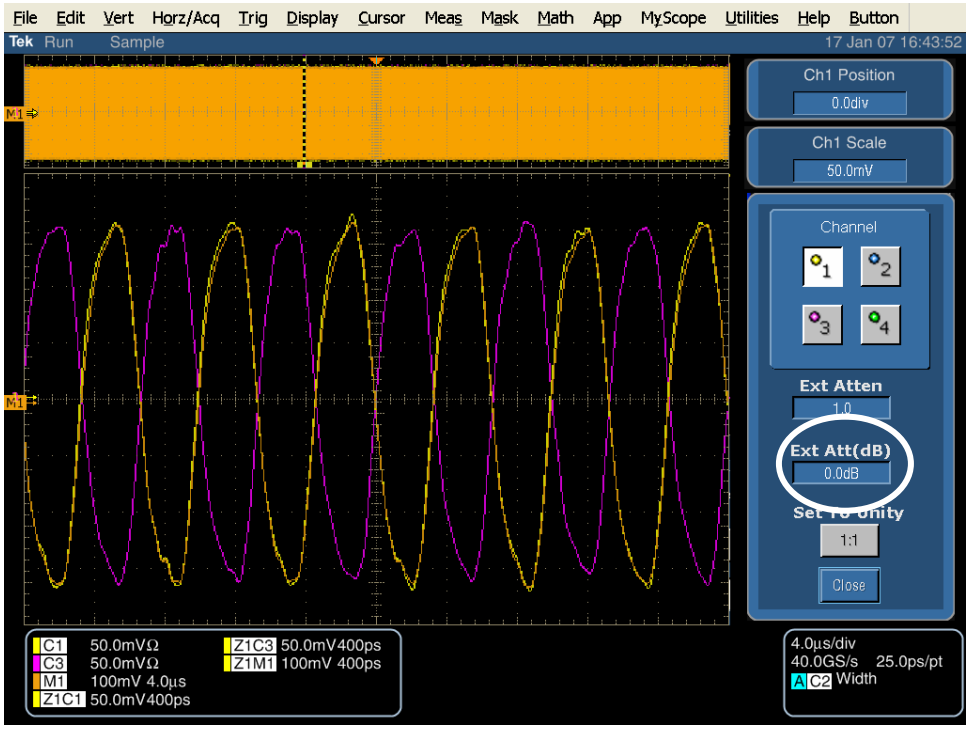
The cursors can be used to mark the 5GHz and 8GHz points on the waveform. Verify that the signal stays below -20dB up to 5GHz, and stays below 10dB from 5GHz to 8GHz.

Once the return loss performance has been verified using the 6dB attenuators, the attenuator values can be entered into the scope vertical setup to automatically adjust the amplitude values for the attenuation.

From the main menu, click on “Vert”.



Click on the Atten button under the “Probe” section.



Enter in the Attenuator value. For example, a 6dB attenuator would be entered as “6.00” in the Ext Att(dB) box. Enhanced accuracy can be attained by characterizing the attenuator on the TDNA system (insertion loss), then entering the measured value of the attenuator.


File Edit Vert Horz/Acq Trig Display Cursor Meas Mask Math App MyScope Utilities Help Button
Tek Run Sample
17 Jan 07 16:44:46
Ext Atten
1.9275
Ext Att(dB)
5.7dB
Channel
Ext Atten
1.9275
Ext Att(dB)
5.7dB
Set To Unity
1:1
Close
C1 50.0mVΩ
C3 50.0mVΩ
M1 100mV 4.0µs
Z1C1 50.0mV400ps
Z1C3 50.0mV400ps
Z1M1 100mV 400ps
4.0µs/div
40.0GS/s 25.0ps/pt
A C2 Width

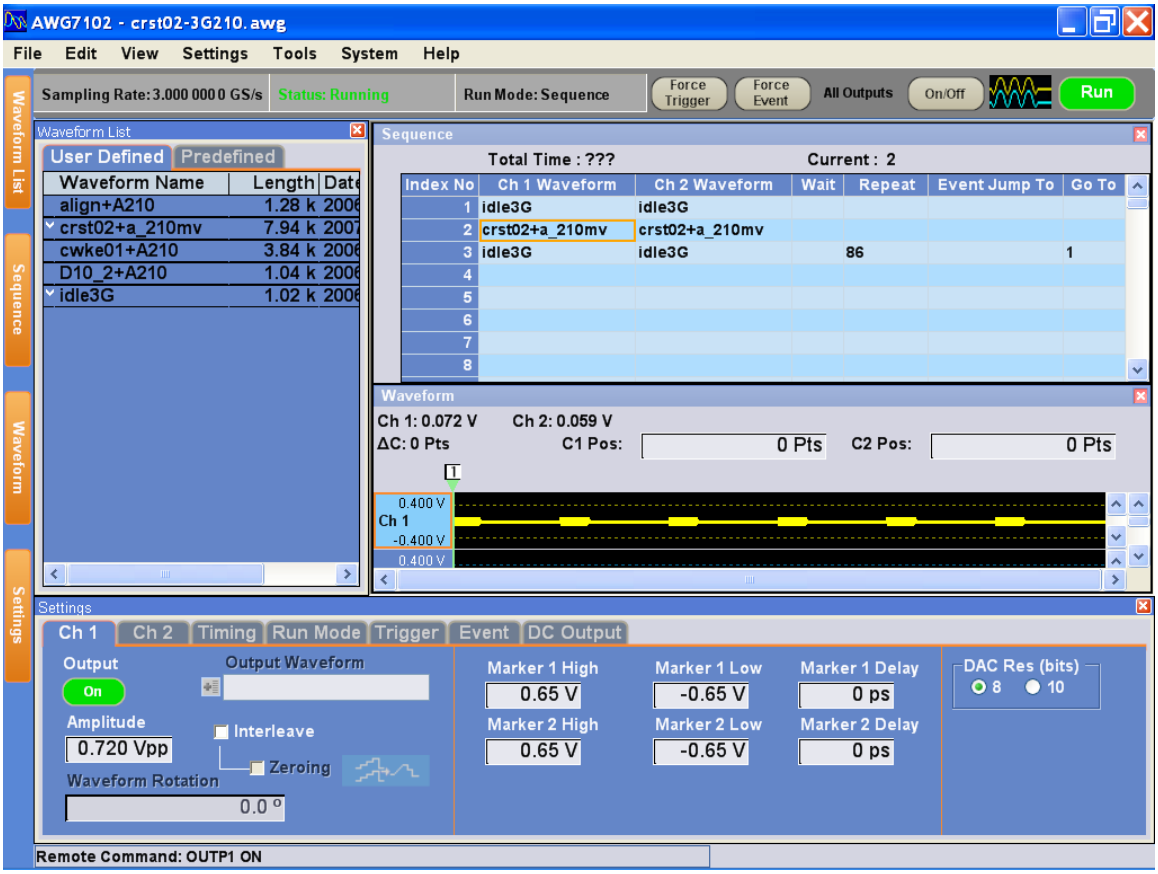
Appendix F – OOB-01 Level Calibration Procedure for AWG7102

This procedure assumes that the scope has been properly set up prior to making any measurements. This includes a 20 minute warm-up, running SPC, applying any required external attenuation, entering the attenuator values into the scope's vertical setup, and performing channel deskew. Once this is done, the scope can be connected to the SATA test fixture.

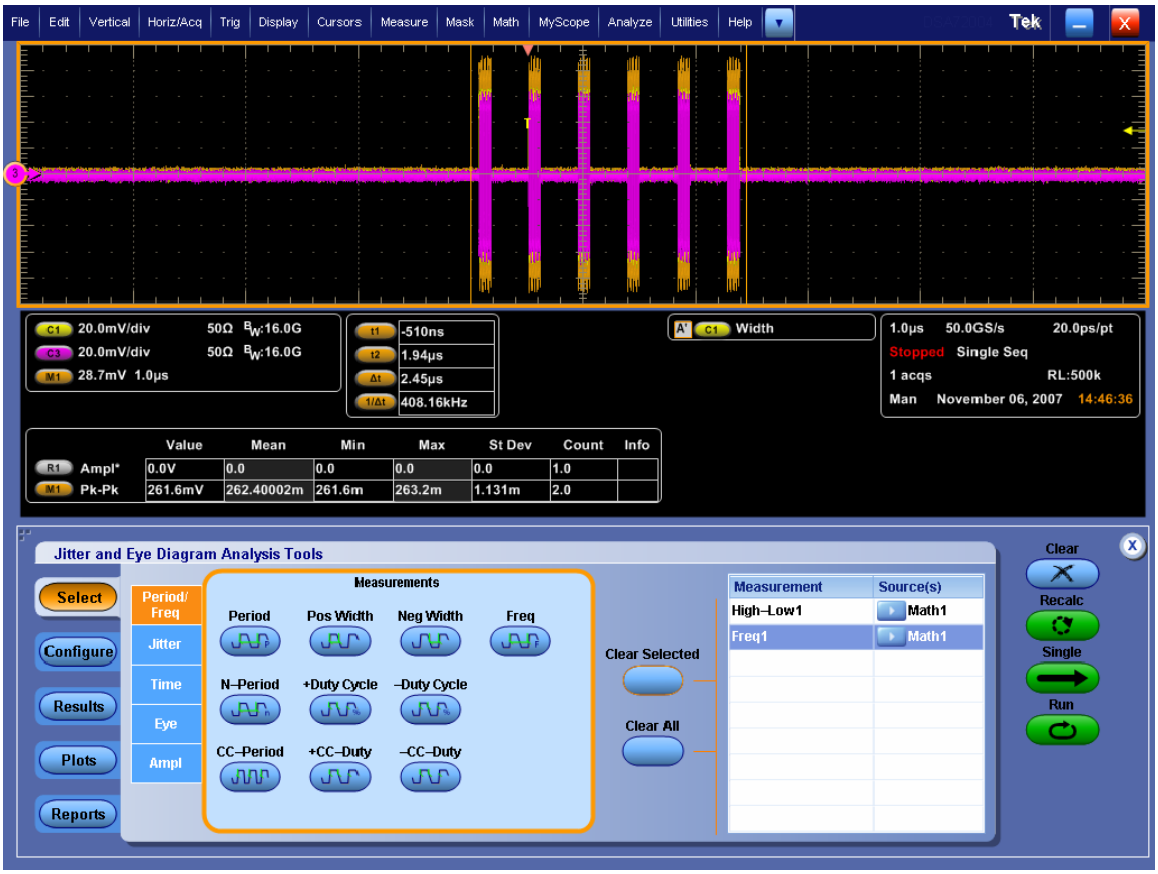
It addition, this procedure assumes that the AWG has been properly set up prior to making any measurements. This includes a 20 minute warm-up, and running the system calibration. Once this is complete, the AWG can be connected to the SATA test fixture.

After the equipment has been properly set up, connect a loop-back to the SATA Near End fixture. This loop-back consists of a SATA Far End fixture, and short SMA cables which connect the Transmitter D+ to the Receiver D+, and the Transmitter D- to the Receiver D-. If a loop-back is not available, it is acceptable to disconnect the SATA test fixture, and connect the Tx and Rx cables together using SMA barrel connectors.

On the AWG, open the "CRST02-3G210.awg" file. This produces an OOB COMINIT/COMRESET burst set that is approximately 210mV in amplitude.



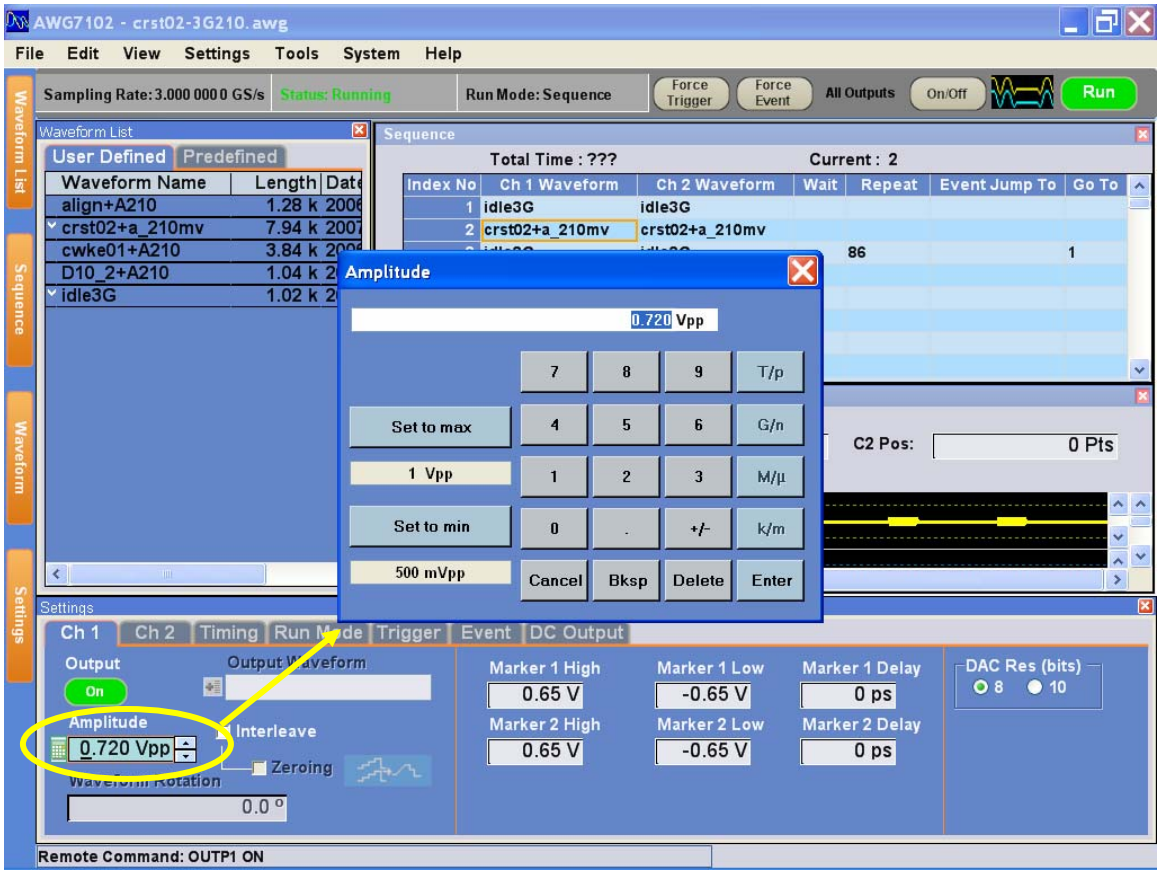
On the scope, launch the Jitter and Eye Analysis package (DPOJET).



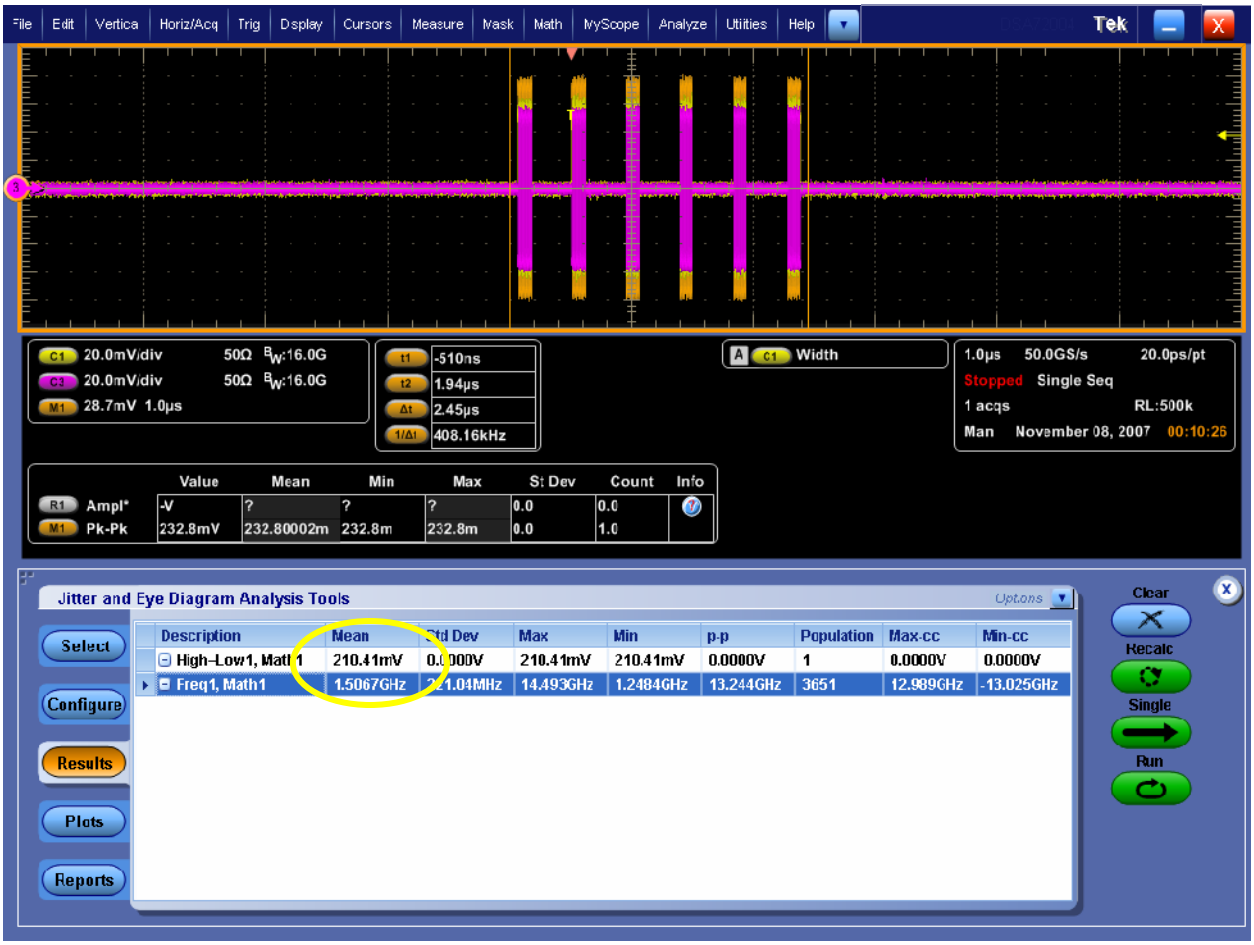
Recall the settings file “SATA OOB 210mv cal”. This will configure the scope as well as the DPOJET settings.

Note that the SATA Logo group has defined this measurement to be made using a MODE measurement on the .45 to .55 (center 10%) portion of the UI, and to average the MODE measurements of all of the UI contained in all of the COMINIT bursts. It is not necessary to manually set the DPOJET settings after loading the settings file, but the following screen shows the settings that are created by the “SATA OOB 210mv cal” setup file:

Click on the “Run” button, and while the measurement is running, adjust the AWG output amplitude as close as possible to 210mV. It might be convenient to stop the measurement, clear the previous data, and restart the data to get a more accurate reading. If everything is configured properly, it will be easy to get better than 1% error (+/- 2mV) on this adjustment. The following screen shows the adjustment window:



The results will be displayed on the scope in the following location:



Repeat the procedure for the 40mV and 60mV settings. The AWG files used to generate the signals are “CRST02-3G040.awg” and “CRST02-3G060.awg”. The setup files for the scope to make these measurements are “SATA OOB 40mv cal.set” and “SATA OOB 60mv cal.set”.

Appendix G – Calibration and Verification of Jitter Measurement Devices

In an effort to get better correlation between different jitter measurement systems, the SATA PHY group has defined a standard jitter transfer function requirement which all jitter measurement systems must meet. This is detailed in ECN-008. The following procedure describes the process for performing the Jitter Transfer Function calibration. This calibration must be done once prior to making TSG-09 through TSG-12.

The response to jitter of the Jitter Measurement Device (JMD)(the reference clock is part of the JMD) is measured with three different jitter modulation frequencies corresponding to the three cases: 1) SSC (full tracking) 2) jitter (no tracking) 3) the boundary between SSC and jitter. The jitter source is independently verified by separate means. This ensures the jitter response of the JMD is reproducible across different test setups.

The three Gen1i test signals are: 1) a 375MHz +/- 0.035% square wave (which is a D24.3, 00110011 pattern) with risetime between 67ps and 136ps 20 to 80% [1] with a sinusoidal phase modulation of 20.8ns +/- 10% peak to peak at 30kHz +/- 1%. 2) a 375MHz square wave with a sinusoidal phase modulation of 200ps +/- 10% peak to peak at 50MHz +/- 1%. 3) a 375MHz square wave with no modulation.

The three Gen2i test signals are: 1) a 750MHz +/- 0.035% square wave (which is a D24.3, 00110011 pattern) with risetime between 67ps and 136ps 20 to 80% [1] with a sinusoidal phase modulation of 20.8ns +/- 10% peak to peak at 30kHz +/- 1%. 2) a 750MHz square wave with a sinusoidal phase modulation of 100ps +/- 10% peak to peak at 50MHz +/- 1%. 3) a 750MHz square wave with no modulation

The independent separate means of verification of the test signals is a time interval error plot on a real time oscilloscope.

The test procedure checks two conditions: the JTF attenuation and the JTF bandwidth. Care is taken to minimize the number of absolute measurements taken, making most relative; this reduces the dependencies and improves accuracy.

The basic procedure is as follows:

1. Adjust the pattern generator for a D24.3 pattern (00110011) (Gen2 is a 750MHz sine wave) and modulation to produce a 30 KHz +/- 1%, 20.8 ns p-p +/- 10% sinusoidal phase modulation.
2. Verify the level of modulation meets the requirements and record the p-p level (DJ t). This is done with a Time Interval Error (TIE) type measurement or equivalent.
3. Apply test signal to the JMD. Turn on the sinusoidal phase modulation. Record the reported DJ.
4. Turn off the sinusoidal phase modulation. Record the reported residual DJ.
5. Calculate and record the level of applied DJ by subtracting the DJ with modulation off from DJ with modulation on.
6. Calculate the jitter attenuation by 20Log(DJ m / DJ t). This value must fall within the range of –72dB +/- 3dB. Adjust the JMD settings to match this requirement.
7. Adjust the pattern generator for a D24.3 pattern (00110011) and modulation to produce a 50 MHz +/-1%, 0.3 UI p-p +/- 10% (200ps for Gen1i or 100ps for Gen2i) sinusoidal phase modulation, also known as periodic jitter, PJ
8. Verify the level of modulation meets the requirements and record the p-p level (DJ t). This is done with a Time Interval Error (TIE) type measurement or equivalent.
9. Apply test signal to the JMD. Record the level as the reference DJ value (DJ 0dB).
10. Calculate the -3dB value: DJ -3dB = DJ 0dB * 10^(-3/20)
11. Adjust the frequency of the DJ source to 2.1MHz. Shift the frequency of the PJ source until the reported DJ difference between PJ on versus PJ off is equal to (DJ -3dB). The PJ frequency is the -3dB BW of the JTF.

12. Adjust the JMD settings to bring the PJ –3dB frequency to 2.1MHz +/- 1MHz. Repeat step 4 through step 12 until both the jitter attenuation and 3dB frequency are in the acceptable ranges.
13. Check the peaking of the JTF. Adjust the pattern generator for a D24.3 pattern and modulation to produce sinusoidal phase modulation at the –3dB frequency and 0.3 UI p-p +/- 10% (200ps for Gen1i or 100ps for Gen2i). Increase the frequency of the modulation to find a maximum jitter; it is not necessary to increase beyond 20MHz. Record the maximum jitter value and frequency.
14. Calculate the JTF Peaking value: 20Log (DJ pkng/ DJ 0dB). Record this value.

Detailed Procedure:
equipment list:

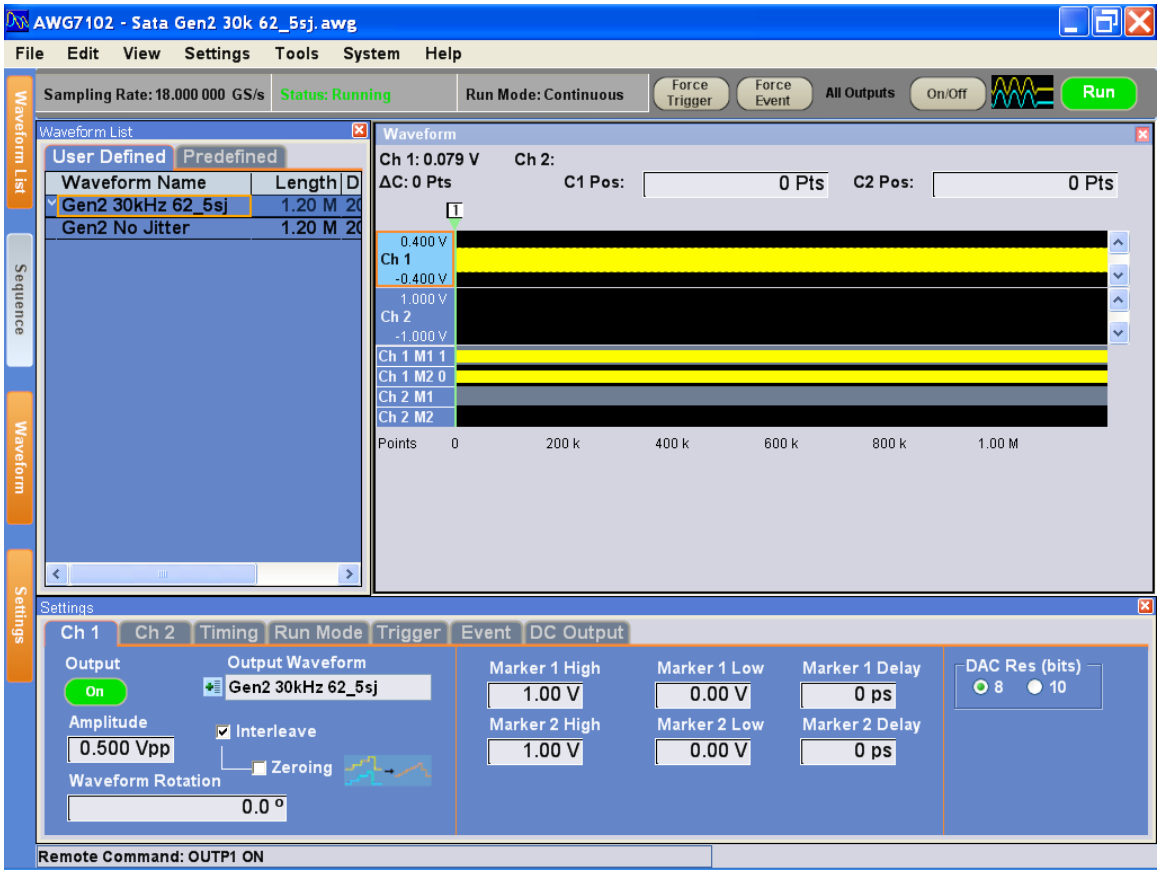
AWG7102 with Opt 6
JTF Waveform Library for AWG7102
test cables
DSA72004 Digital Phosphor Oscilloscope 20GHz, 50G/s, or desired BW
JIT3 software and associated JTF setup files

Step 1: Adjust the pattern generator for a D24.3 pattern (00110011)(MFTP) and modulation to produce a 30 KHz +/- 1%, 20.8 ns p-p +/- 10% sinusoidal phase modulation. To do this on the AWG7102, follow steps "a" through "c" below. Open the waveform file "SATA Gen1 30k 62_5Sj.awg" or "SATA Gen2 30k 62_5Sj.awg" as appropriate. This will set all parameters of the AWG.

a) Connect the AWG to the scope, using the same matched cable set that will be connected to the scope during normal jitter measurements. Verify that the cables are connected to the AWG Interleaved outputs.

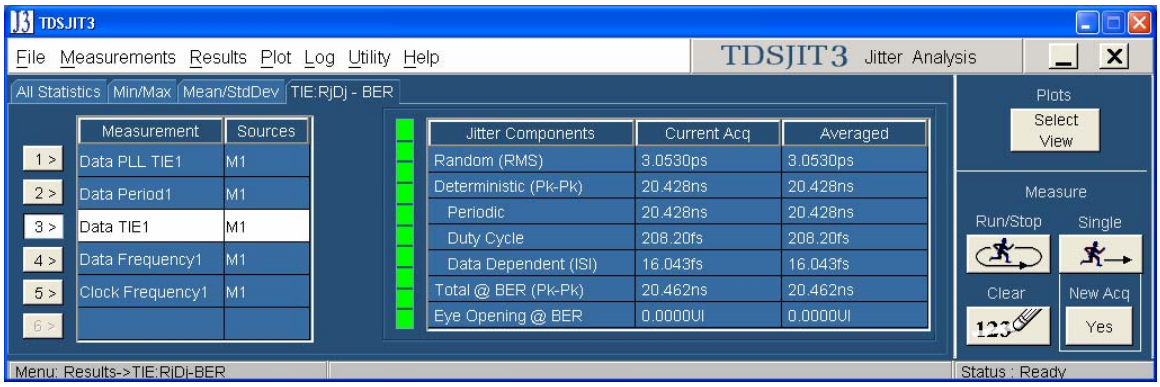
b) Open the waveform file "SATA Gen1 30k 62_5Sj.awg" or "SATA Gen2 30k 62_5Sj.awg" as appropriate Select the "Gen1 30kHz 62_5sj" or "Gen2 30kHz 62_5sj" waveform from the Waveform List on the left side of the display. Drag this to the Waveform display window, and drop in the CH1 area. When the pop-up appears, choose "Set Waveform".

c) Set the AWG output to "On". This will apply the MFTP pattern containing a 30kHz modulation with 20.8ns of jitter to the scope.



Step 2: Verify the level of modulation meets the requirements and record the p-p level (DJ t). This is done with a Time Interval Error (TIE) type measurement or equivalent.

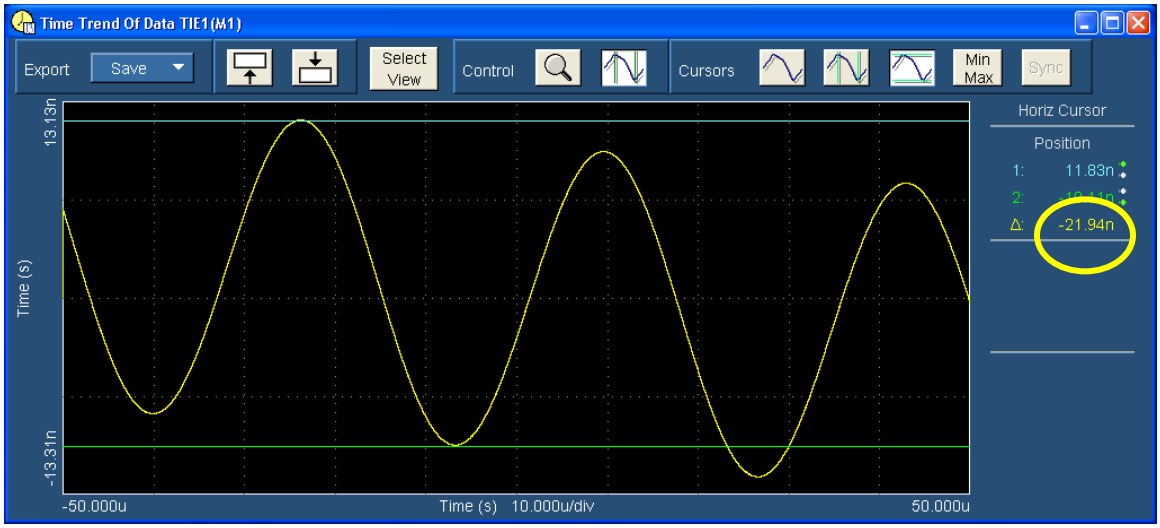
a) Launch the Jitter Analysis (TDSJIT3) application under the Analyze menu on the scope.
b) Recall JIT3 settings file "JTF JIT3 Gen1 setup.ini" or "JTF JIT3 Gen2 setup.ini". This will set up the scope channels as well as the JIT3 settings. It will set up all needed measurements within JIT3. Reference levels will be set automatically when the measurement is run. Click on the "TIE RjDj-BER" tab, and then click on "Data TIE 1". Click on "Single" to run the measurement.



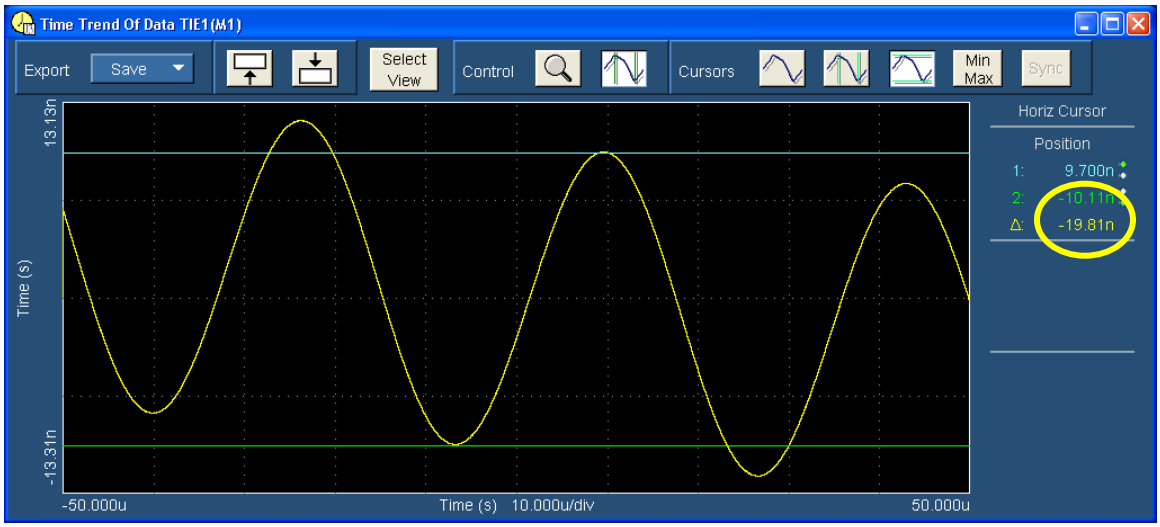
JIT3 produces a measurement for Dj in the statistics table, however this value cannot be used directly.

The setup file has automatically created several plots. Click on the "Select View" button on the right side of the screen, and select the Data TIE1 Trend Plot. The resulting plot of a sine wave pattern may have a long slope which is due to offset values (initial conditions) which are integrated. The peak to peak value of the sinusoidal wave is of importance as this is the level of phase modulation. The long slope needs to be removed from the plot to find the accurate peak to peak phase modulation. To do this, use the cursors to take the average of two peaks vs one valley thus eliminating the long slope.

Choose two adjacent peaks and the valley between to make the measurement. Place horizontal cursors on the trend plot, and position the cursors to the top of the first peak and the valley. Record the measured delta.



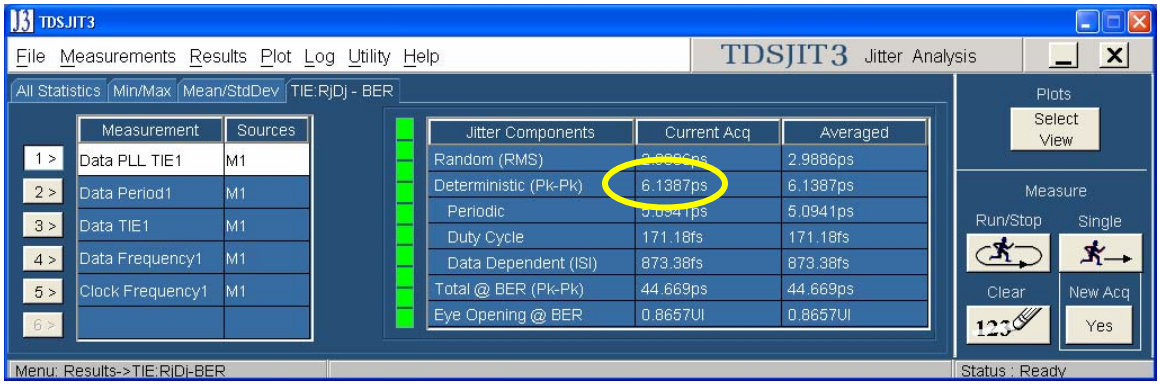
Next, move the top cursor to the second peak, and again record the measured delta.



In this example, peak 1 is 21.94nS, and peak 2 is 19.81nS. The valley is the reference value.
Determine the slope corrected Dj value: (21.94+19.81)/2 = 20.88ns. This verifies the level of phase modulation required. This measured value from the TIE agrees with the level set in the source. Record this value in the JTF Calibration spreadsheet.

Step 3: Apply test signal to the JMD.

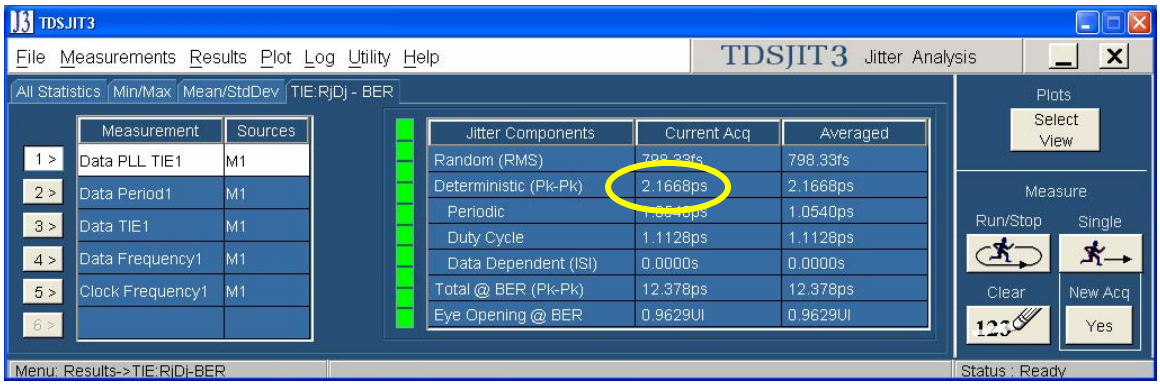
To make the JMD measurement on the 30kHz modulated signal, simply click on the Data PLL TIE 1 measurement in the JIT3 measurement list. It is not necessary to click on the "Single" button to acquire another waveform, as the measurement was made on the last waveform acquired.



Record this measured value in the JTF Calibration spreadsheet.

Step 4: Next, measure the residual jitter. This is done by turning off the 30kHz modulation, and making another jitter measurement. On the AWG, drag the "Gen1 No Jitter" or "Gen2 No Jitter" waveform from the waveform list to the waveform display area, and drop in CH1. When the pop-up window appears, select "Set Waveform". Turn the AWG Ch1 output on.

On the scope, simply click on the "Single" button to make another acquisition.

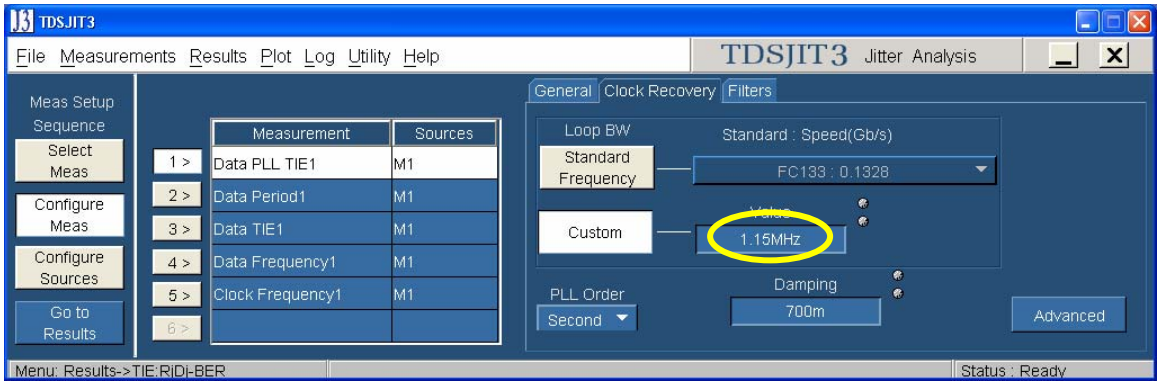


Record this measurement in the JTF Calibration spreadsheet.

The spreadsheet now has enough data to calculate the attenuation level of the JMD.

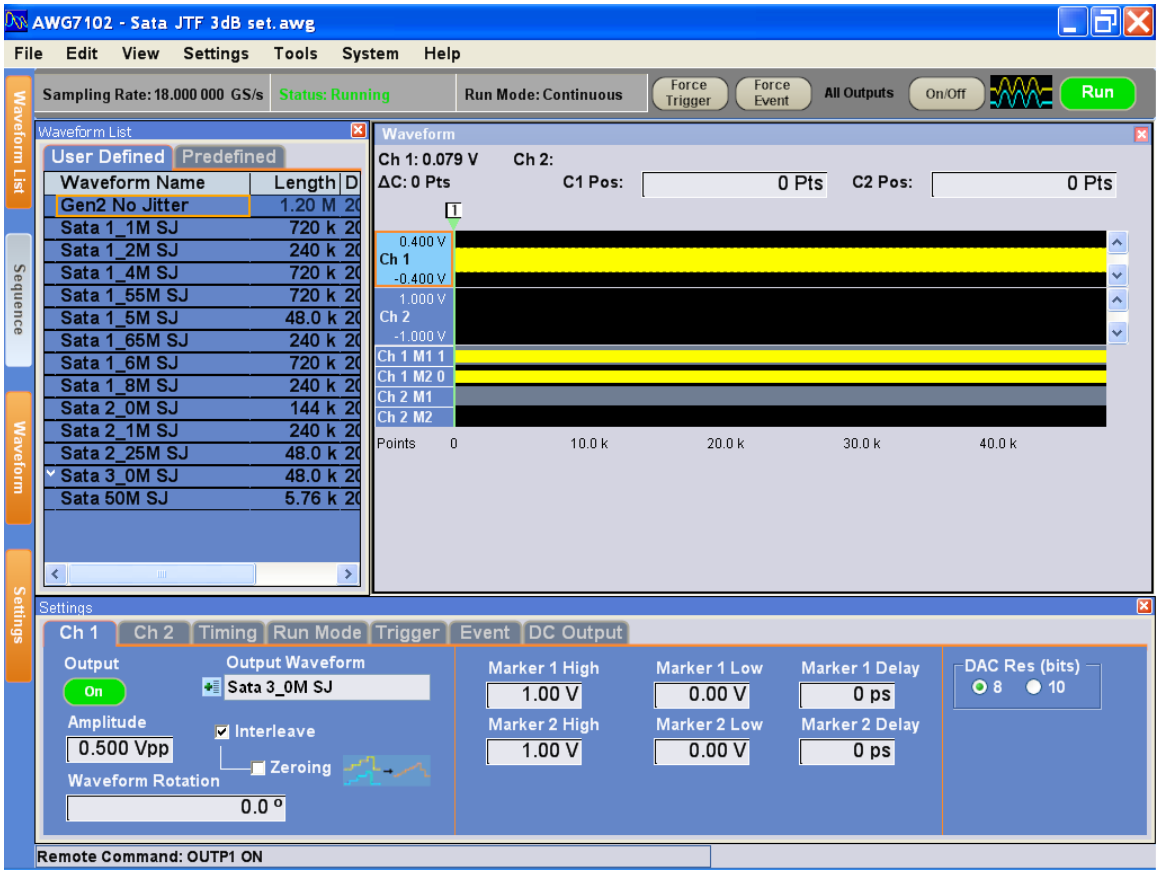
Step 5: The spreadsheet calculates the level of applied DJ by subtracting the DJ with modulation off from DJ with modulation on. (e.g. 6.1387pS - 2.1668pS = 3.9719pS)

Step 6: Calculate the jitter attenuation by 20Log(DJ m / DJ t). This value must fall within the range of –72dB +/- 3dB. Adjust the JMD loop bandwidth setting under the Clock Recovery setup to meet this requirement. (e.g. 20 Log (3.9719pS / 20.83nS) = -74.41dB)

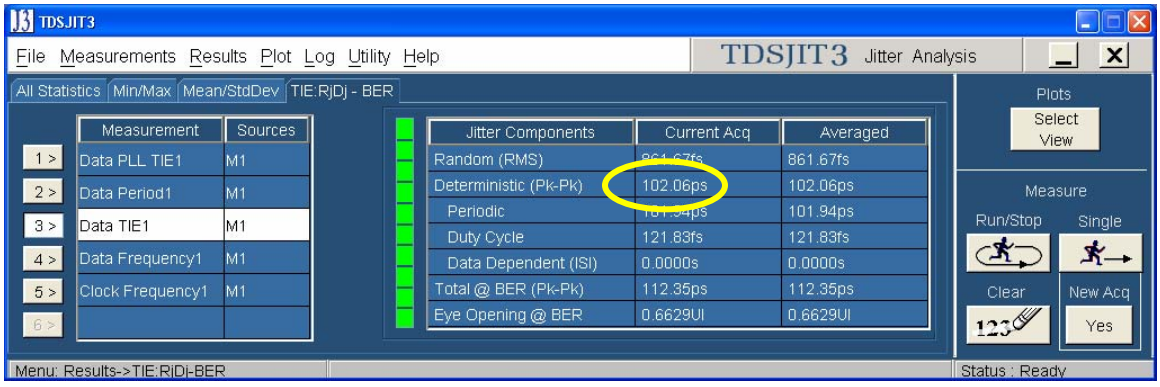


If the calculated attenuation is below -72dB, decrease the loop bandwidth setting, and repeat the process from step 1 to 6 until the required attenuation is attained. **Once the proper loop bandwidth has been determined, use this value setting for all subsequent jitter measurements .**

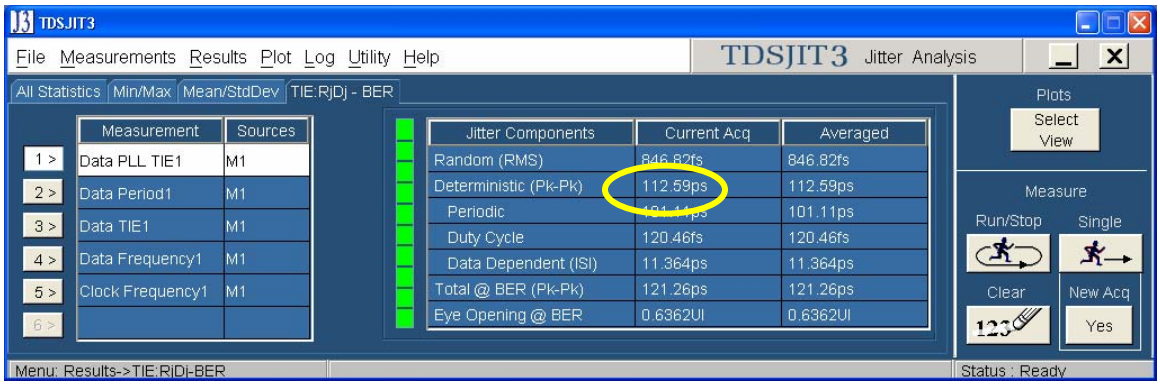
Step 7: Adjust the pattern generator for a D24.3 pattern (00110011) and modulation to produce a 50 MHz +/-1%, 0.3 UI p-p +/- 10% sinusoidal phase modulation. To do this on the AWG7102, open the waveform file “SATA Gen1 JTF 3db set.awg” or “SATA Gen2 JTF 3db set.awg”. This will set all parameters of the AWG. This setup file includes a collection of waveforms that can be used to verify the -3dB point on the jitter transfer curve.



Step 8: Select the SATA 50M SJ waveform from the waveform list. On the scope, click on "Single" to run the acquisition and measurement on JIT3. Click on the DATA TIE 1 measurement, and record the measured Dj. Verify the level of modulation meets the requirements and record the p-p level (DJ t) in the JTF Calibration spreadsheet.



Next, click on the "Data PLL TIE 1" in the measurement list, and record the measured Dj in the JTF Calibration spreadsheet.



Step 9: Next, on the AWG, select the waveform "Gen1 No Jitter" or "Gen2 No Jitter". This is used to verify the residual jitter at this setting.

Again measure and record the Data PLL TIE 1 Dj using JIT3.

This establishes the reference DJ value of excitation that is applied to the JMD. Record the measured jitter level as the reference DJ value (DJ 0dB).

Step 10: The JTF Calibration spreadsheet then calculates the -3dB value: DJ -3dB= DJ 0dB* 0.708.

Step 11: The next step is to determine the specific frequency that matches the -3dB level found in step 10. This is done by sequentially setting the AWG Dj frequency in a range from 1.1MHz to 3MHz. At each setting, the measurement is made on the scope using the Data PLL TIE 1 measurement. Assume the residual DJ is zero for the search (this speeds up the search).

Once the -3dB frequency is determined, record the measured Dj at that frequency into cell B13 of the JTF Calibration spreadsheet. Next, turn off the jitter modulation on the AWG by again selecting the Gen2 No Jitter waveform. Retake the measurement to get the residual, and enter this into the spreadsheet at cell B14. Enter the -3dB frequency in spreadsheet cell B15.

Step 12: Verify the DJ –3dB frequency is 2.1MHz +/- 1MHz. The typical -3dB frequency is approximately 1.55MHz. Repeat step 4 through step 12 until both the jitter attenuation and 3dB frequency meet the requirements of the specifications contained in ECN-008.

Step 13: Next, check the peaking of the JTF. Adjust the pattern generator for a D24.3 pattern and modulation to produce sinusoidal phase modulation at the –3dB frequency and 0.3 UI p-p +/- 10%. This is done on the AWG by opening the file "Sata Gen1 JTF peak set.awg" or "Sata Gen2 JTF peak set.awg". This provides waveforms containing the prescribed amount of jitter at frequencies ranging from 3MHz to 20MHz.

To find the peaking of the JTF requires multiple jitter measurements which may be time consuming. The JTF peaking is flat over a portion of the range. Start at the 3dB frequency setting, and increment by 1MHz until reaching 20MHz or the readings start to decrease. Record the maximum jitter value and frequency. Once the peaking frequency is determined, enter the Dj value measured at that frequency into the spreadsheet at cell B16. Again determine the residual level by turning off the jitter on the AWG, and enter that measured residual jitter into the spreadsheet at cell B17. Enter the peaking frequency at cell B18 of the spreadsheet.

Step 14: The spreadsheet provides a calculation of the peaking level using the formula: 20*log(Dj-peaking/Dj-0dB)

Typical peaking for the Tek system is 3MHz. The following is a completed example spreadsheet:

	Cal performed on 11/06/07 using Dj (pp)								
	Recorded Values		Calculated Values		Calculated Values	Hi Lim	Lo Lim	Result	Notes
Data Frequency	7.5000E+08					7.5026E+08	7.4974E+08	PASS	
SSC Frequency	3.0010E+04					3.0300E+04	29700	PASS	
	Tj	20.837e-9	Rj	2.0625e-12					
DJSSC, applied PM at 30kHz	2.1518E-08					2.288E-08	1.872E-08	PASS	Measured using DATA TIE with no PLL or filtering applied
DJSSCON, measured jitter at 30kHz	6.43E-12								Loop bandwidth set to 1.12MHz
DJSSCOFF, measured residual jitter at 30kHz	1.94E-12	**DJMSSC**	4.494E-12	**Attenuation**	-73.602604	-69	-75	PASS	If this number does not come out very close to -72, adust the loop bandwidth, and test again
DJM, applied jitter at 50MHz	1.0205E-10					1.100000E-10	9.000000E-11	PASS	50M jittered signal Measured using DATA TIE with no PLL or filtering applied
DJMON, measured jitter at 50MHz	1.1266E-10								50M jittered signal measured using DATA PLL TIE
DJMOFF, measured residual jitter at 50MHz	1.7457E-12	**DJMM**	1.109E-10	**DJ3DB**	7.8416E-11				Measure the residual again by setting source to no jitter 3dB down Level in cell F12
DJON, measured jitter at 3dB point	8.1445E-11								
DJOFF, measured residual jitter at 3dB point	1.7787E-12	**DJ**	7.967E-11						Adjust the input Sj frequency until this number matches the value shown in cell F12
F3DB, 3dB frequency	1.55E+06					3.10E+06	1.10E+06	PASS	Note: -3db actually likely to be 1.525 or 1.53MHz
DJPKON, measured jitter at peaking frequency	1.34E-10								Now sweep the Sj freq from 1MHz to 20MHz, and find the highest PLL TIE jitter value. Record here.
DJPKOFF, measured residual jitter at peaking frequency	1.9494E-12	**DJPK**	1.323E-10	**Peaking:**	1.53	dB Peaking			
FPK, peaking frequency	3.00E+06								